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(71) Applicant: **SANYO ELECTRIC Co., Ltd.**
Moriguchi-shi, Osaka 570 (JP)

(72) Inventor: **TOGUCHI, Akira**
Osaka 574 (JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
80058 München (DE)

(54) METHOD AND APPARATUS FOR ENCODING

(57) An encoder includes a control bit insertion circuit (12) for inserting a control bit into input data, which is then subjected to I-NRZ modulation by a precoder (14) to generate a reference code. The reference code is given to a 4-code generation circuit (22) through a delay circuit (16), and frequency components of the reference code, and first, second and third codes generated on the basis of the reference code are detected by a frequency detector (18). The frequency components are given to a judge circuit (20) such that it is determined whether the frequency components are large or small. A judge signal is applied to the 4-code generation circuit and a frequency detector from the judge circuit. The 4-code generation circuit selectively outputs one selected from the reference code and the first to third codes on the basis of the judgement signal.

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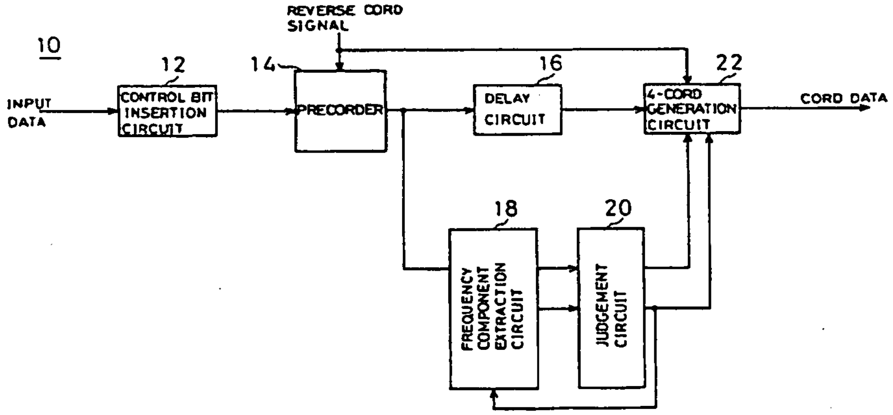
REVERSE CORD SIGNAL
10
12
14
16
22
INPUT DATA
CONTROL BIT INSERTION CIRCUIT
PRECORDER
DELAY CIRCUIT
4-CORD GENERATION CIRCUIT
CORD DATA
18
20
FREQUENCY COMPONENT EXTRACTION CIRCUIT
JUDGEMENT CIRCUIT

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Description

FIELD OF THE INVENTION

The present invention relates to a coding method and apparatus. More specifically, the present invention realtes to a coding method and apparatus used for a VTR, VCR, and etc.. adopting a digital pilot signal recording system so as to convert input data to which a control bit is added at a head into an output code.

PRIOR ART

One example of conventional such a kind of coding apparatus is disclosed in, for example, Japanese Patent Application Laying-open No. 4-255969 [G11B20/14, H03M7/30] laid-open on September 10, 1992. In the prior art, frequency components of two kinds of codes obtained by inserting a control bit of "0" or "1" at a head of input data of N+1 bits and by subjecting the same to I-NRZ modulation, and an appropriate code is selectively outputted through comparison of processed results, and last two bits of a selected code to a precoder for the I-NRZ modulation of next input data.

Since in such a prior art coding apparatus, the last two bits of the output code are fed-back, it is necessary to process preceding input data within a time that the input data equal to one code is modulated, e.g. a time period of 25 clocks in a case where one code is 25 bits so as to output the appropriate code, it is difficult to put the coding apparatus into practical use. More specifically, since a frequency component extraction circuit performs Fourier transform for a DC component and components of frequencies f1 and f2 in a modulated code, a circuit becomes quite large and a processing time for the extraction of the frequency components becomes long, it is quite difficult to shorten a time period to extract the frequency components for one bit in comparison with a time period for the I-NRZ modulation of one bit data, therefore, and accordngly, it is difficult to put the coding apparatus into practical use.

SUMMARY OF THE INVENTION

Therefore, a principal object of the present invention is to provide a novel coding mathod.

Another object of the present invention is to provide a coding method in which it is unnecessary to feed-back a portion of a preceding code.

A further object of the present invention is to provide a coding apparatus which implements the above described coding method.

According to the present invention, a coding method comprises steps of: (a) inserting a control bit into input data; (b) generating a reference code on the basis of input data into which the control bit is inserted; (c) generating a predetermined number of associate codes on the basis of the reference code; and (d) selectively outputting one of the reference code and the associate codes on the basis of frequency components of the reference code and the associate codes.

According to the present invention, a coding apparatus comprises: insertion means (12) for inserting a control bit into input data; reference code generation means (14) for generating a reference code on the basis of data outputted from the insertion means; associate code generation means (22, 56a, 56b, 56c) for generating a predetermined number of associate codes being in correlation with the reference code on the basis of the reference code; judgment signal output means (18, 20) for outputting a judgment signal on the basis of frequency components of the reference code and the associate codes; and code output means (22, 54) for selectively outputting one of the reference code and the associate codes according to the judgment signal.

In accordance with the present invention, since the associate codes are generated in advance on the basis of the reference code, and one code is selectively outputted on the basis of the frequency components of these codes, it is unnecessary to feed-back last two bits of a preceding output code, and therefore, a time restriction is released, and accordingly, it is possible to certainly convert the input data into the code.

In one embodiment, the judgment signal output means includes first to N-th extraction means for extracting first to N-th (N is an integer) frequency components of each of the reference codes and the associate codes, first to N-th calculation means for calculating each of the first to N-th frequency components, and outputting first to 2^M-th (M is a positive integer) calculation results, and first to 2^M-th operation means for operating each of the first to 2^M-th calculation results outputted from the first to N-th calculating means.

In a case where frequency components are processed at every one code (in a case where M = 1), frequency components of the reference code and a first to third codes (the associate codes) generated on the basis of the reference code are extracted by frequency component extraction circuits, two of these frequency components are applied to a first and second component addition circuits included in, for example, a DC component extraction circuit. Then, the first addition circuit functions as first, second, third and fourth addition means, and the second addition circuit functions as fifth, sixth, seventh and eighth addition means in accordance with a change-over switch, for example. Therefore, the frequency components are added each other, and outputs of the first addition circuit and the second addition circuit are outputted from a DC component calculation circuit as the first calculation result and the second calculation result. These process is executed in the other calculation circuits, e.g. f1 sine component extraction circuit, f1 cosine component extraction circuit, f2 sine component extraction circuit and f2 cosine component extraction circuit. Then, the first calculation result and the second calculation result outputted from the calculation circuits are operated by a first square waiting addition circuit and a second square waiting addition circuit, respectively, and the operation results are applied to the judgment circuit. The judgment circuit judges sizes of the operation results, and outputs a judgment signal according to the sizes. The reference code is converted into a predetermined output code by, for example, a 4-code generation circuit according to the judgment signal.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an illustrative view showing an operation of an I-NRZ modulation.
Figure 2 is an illustrative view showing an operation of the I-NRZ modulation;
Figure 3 is an illustrative view showing an operation of the I-NRZ modulation;
Figure 4 is a block diagram showing one embodiment according to the present invention;
Figure 5 is a block diagram showing a portion of Figure 4 embodiment;
Figure 6 is a block diagram showing a portion of Figure 4 embodiment;
Figure 7 is a block diagram showing a portion of Figure 4 embodiment;
Figure 8 is a block diagram showing a portion of Figure 4 embodiment;
Figure 9 is a block diagram showing a portion of Figure 4 embodiment;
Figure 10 is a block diagram showing a portion of Figure 4 embodiment;
Figure 11 is a block diagram showing a portion of Figure 4 embodiment;
Figure 12 is an illustrative view showing a portion of an operation of Figure 4 embodiment;
Figure 13 is a block diagram showing a portion of Figure 4 embodiment;
Figure 14 is a block diagram showing a portion of Figure 4 embodiment;
Figure 15(A) is an illustrative view showing an output of a precoder, Figure 15(B) is an illustrative view showing an output of a hold circuit, Figure 15(C) is an illustrative view showing an output of a judgment circuit, and Figure 15(D) is an illustrative view showing an output of a 4-code generation circuit;
Figure 16 is an illustrative view showing a portion of the operation of Figure 4 embodiment;
Figure 17 is an illustrative view showing a portion of the operation of Figure 4 embodiment;
Figure 18 is an illustrative view showing a portion of Figure 4 embodiment;
Figure 19 is a waveform chart showing a frequency spectrum of a record signal;
Figure 20 is a block diagram showing another embodiment according to the present invention;
Figure 21 is a block diagram showing a portion of Figure 20 embodiment;
Figure 22 is a block diagram showing a portion of Figure 20 embodiment;
Figure 23 is a block diagram showing a portion of Figure 20 embodiment;
Figure 24 is a block diagram showing a portion of Figure 20 embodiment;
Figure 25 is a block diagram showing a portion of Figure 20 embodiment;
Figure 26 is a block diagram showing a portion of Figure 20 embodiment; and
Figure 27(A) is an illustrative view showing an output of a precoder, Figure 27(B) is an illustrative view showing an output of a hold circuit, Figure 27(C) is an illustrative view showing an output of a judgment circuit, and Figure 27(D) is an illustrative view showing an output of a 4-code generation circuit.

BEST MODE FOR EMBODYING THE INVENTION

An embodiment described in the following utilizes facts that the number of the kinds of codes generated in claim by inserting "0" or "1" as a control bit into input data and subjecting to I-NRZ modulation is always limited to four (4) for the same input data, and that the four kinds of codes have a specific relationship to each other can be generated from one kind of code, and that there is a predetermined rule in the relationship of the four kinds of codes.

The facts will be described with referring to Figure 1 and Figure 2. As shown in Figure 1(A) and Figure 1(B), in a code A0 obtained by inserting "0" as the control bit into input data "a" of 24 bits and subjecting inserted data to the I-NRZ modulation and a code A1 obtained by inserting "1" as the control bit into the input data "a" and subjecting inserted data to the I-NRZ modulation, bits of odd numbers of the codes A0 and A1 have an inverted relationship. This means that second bits in the last two bits of each code have the inverted relation. The last two bits become first two bits of a modulation signal used for the next I-NRZ modulation. Furthermore, as understood from Figure 2(A) and Figure 2(C), in a code B0 obtained by inserting "0" into succeeding 24 bits of input data "b" and subjecting inserted data to the I-NRZ modulation at a time that a preceding code is a code obtained by inserting "0" (the last two bits are "00") and a code B2 obtained by inserting "0" into succeeding input data "b" and subjecting inserted data to the I-NRZ modulation at a time that a preceding code is a code obtained by inserting "1" (the last two bits are "01") bits of even numbers of the codes B0 and B2 have the inverted relationship.

Furthermore, as understood from Figure 2(B) and Figure 2(D), in a code B1 obtained by inserting "1" into succeeding input data "b" and subjecting inserted data to the I-NRZ modulation at a time that a preceding code is a code obtained by inserting "0" and a code B3 obtained by inserting "1" into succeeding input data "b" and subjecting inserted data to the I-NRZ modulation at a time that a preceding code is a code obtained by inserting "1", bits of even number of the codes B1 and B3 have the inverted relationship.

Furthermore, as understood from Figure 2(A) and Figure 2(D), all bits of the codes B0 and B3 have the inverted relation in the code B0 obtained by inserting "0" into succeeding input data "b" and subjecting inserted data to the I-NRZ modulation at a time that a preceding code is a code obtained through the "0" insertion and the code B3 obtained by inserting "1" into succeeding input data "b" and subjecting inserted data to the I-NRZ modulation at a time that a preceding code is a code obtained through the "1" insertion.

In the following description, a code obtained by inserting "0" as the control bit and subjecting to the I-NRZ modulation is regarded as a reference code S0 (or an S0 code), a code that odd number bits have the inverted relation to with respect to odd number bits of the S0 code is regarded as an S1 code, a code that even number bits have the inverted relation with respect to even number bits of the S0 code is regarded as an S2 code, and a code that all bits have the inverted relation to all bits of the S0 code is regarded as an S3 code. Since this relation is the same in the last two bits of the S0 code to the S3 code, a result obtained by inserting "0" into 24 bits following the S0 code and subjecting to the modulation and a result obtained by inserting "1" into 24 bits following the S2 code and subjecting to the modulation become the same, and a result obtained by inserting "1" into 24 bits following the S0 code and subjecting to the modulation and a result obtained by inserting "0" into 24 bits following the S2 code and subjecting to the modulation become the same. Furthermore, a result obtained by inserting "0" into 24 bits following the S1 code and subjecting to the modulation and a result obtained by inserting "1" into 24 bit following the S3 code and subjecting to the modulation are the same, and a result obtained by inserting "1" into 24 bits following the S1 code and subjected to the modulation and a result obtained by inserting "0" into 24 bits following the S3 code and subjecting to the modulation are the same.

That is, as a result that three data sequentially inputted are subjected to the I-NRZ modulation in chain, eight (8) codes can be obtained at a third time; however, it is finally no more than that two couples of four kinds of codes can be obtained. Codes which can be obtained in a following data chain are always limited to four kinds of codes S0 to S3 defined in the above description. Furthermore, codes linked to the S0 code or the S2 code are the S0 code and the S1 code in the four kinds of codes, and codes linked to the S1 code or the S3 code are the S2 code and the S3 code.

Accordingly, in the four kinds of code obtained by subjecting an input data train, a code obtained by inserting "0" as the control bit and subjecting to the I-NRZ modulation is regarded as a reference code A0 (or an A0 code), a code that odd number bits have the inverted relationship to that of the A0 code is regarded as an A1 code, a code that even number bits have the inverted relationship to that of the A0 code is regarded as an A2 code, and a code that all bits have the inverted relationship to that of the A0 code is regarded as an A3 code, and if coefficients of "0" to "3" are to be added to sides of B, C, D in the same manner in succeeding input data "b", "c" and "d", chain relationship of the codes are shown in Figure 3.

An embodiment described in the following is an embodiment in which a time restriction during in processing frequency components as in the prior art can be removed because it is possible to estimate the four kinds of codes from one kind of code and the chain relationship between a preceding code and a succeeding code is known in advance.

In the following, a case that the input data is processed at every one code (a case of M = 1) and a case that the input data is processed at every two codes having the chain relationship will be described with assuming that a period necessary for an operation for extracting a frequency component is 25 clocks and that a period necessary for an operation of calculation and judgment following the extraction operation is 15 clocks. First, the case that the input data is processed at every one code is described.

With referring to Figure 4, a coding apparatus 10 of this embodiment includes a control bit insertion circuit 12 by which the control bit "0" of 1 bit is inserted into the input data of 24 bits. Data into which the control bit is inserted is then subjected to the I-NRZ modulation in a precoder 14, whereby the reference code S0 is generated. In addition, an inverted code signal is inputted into the precoder 14, and an operation of the precoder 14 is changed in accordance with a level of this signal.

The reference code S0 outputted from the precoder 14 is succeedingly applied to a delay circuit 16 and a frequency component extraction circuit 18. The frequency component extraction circuit 18 generates the S0 code to the S3 code on the basis of the reference code S0, and outputs frequency component extraction results of two codes in the S0 code to the S3 code on the basis of a judgment result of the preceding or last code. The judgment circuit 20 judges the extraction result smaller than the other result, and outputs a judgment signal of a high level or a low level in response to a judgment result for a 4-code generation circuit 22 and the frequency component extraction circuit 18. In addition, a judgment signal according to the preceding or last judgment is also outputted from the judgment circuit 20 to the 4-code generation circuit 22 simultaneously.

The reference code S0 inputted into the delay circuit 16 is delayed for a time period (40 clocks) till the judgment selection signal is outputted from the judgment circuit 20, and then applied to the 4-code generation circuit 22. The 4-code generation circuit 22 selects to output a desired code out of the reference code S0 and the S1 code to the S3 code generated according to the code S0. In addition, an inverted code signal is also applied to the 4-code generation circuit 22, whereby an operation of the 4-code generation circuit 22 is changed. An outputted code is recorded into a magnetic tape 60 (Figure 18) as described later.

Constitution of the precoder 14 is shown in Figure 5. The control bit and a first bit of the input data into which the control bit is inserted is inputted to one terminals of switches 24a and 24b each of which is controlled by the inverted code signal, and a second bit to a twenty-fourth bit of the input data are applied to one terminals of EXOR circuits 26c to 26y, respectively. Furthermore, output signals from latch circuits 28a and 28b outputs of which are controlled by a last two bits hold signal are applied to other terminals of the switches 24a and 24b, respectively. Then, the control bit and the first bit of the input data are outputted from the switches 24a and 24b when the inverted code signal is a low level, and the outputs of the latch circuit 28a and 28b are outputted therefrom when the inverted code signal is a high level, and then, the outputs are applied to the one terminals of the EXOR circuits 26a and 26b, respectively. A first bit of the reference code S0 is applied to the other terminal of the EXOR circuit 26c, and a second bit of the reference code S0 is applied to the other terminal of the EXOR circuit 26d. In the same manner, each of the outputs of the EXOR circuits is applied to the other terminal of each of the EXOR circuits for a bit two bits later till the EXOR circuit 26x. However, output bits of the EXOR circuits 26x and 26y are latched by the latch circuits 28a and 28b, respectively, and outputs thereof are controlled in accordance with the last two bits hold signal. In addition, the inverted code signal becomes a low level when the input data is normal data, and the inverted code signal becomes a high level when the input data is particular data used for a synchronization signal area, an overwrite margin area, and etc.

Constitution of the frequency component extraction circuit 18 is shown in Figure 6. The S0 code outputted from the precoder 14 is applied to a DC component calculation circuit 30a which operates as a Fourier transform circuit, a frequency f1 sine component calculation circuit 30b, a frequency f1 cosine component calculation circuit 30c, a frequency f2 sine component calculation circuit 30d and a frequency f2 cosine component calculation circuit 30e. Then, the S1 code to the S3 code are generated on the basis of the S0 code, and thereafter, a sine component and a cosine component of each of the S0 code and the S1 code or each of the S2 code and the S3 code are calculated in accordance with the judgment signal, and the calculation results are outputted. S0 associate calculation results or S2 associate calculation results out of the count results outputted from the calculation circuits 30a to 30e are applied to a square weighting addition circuit 32a, and S1 associate calculation results or S3 associate calculation results therein are applied to a square weighting addition circuit 32b. Then, an addition results is outputted from each of the square weighting addition circuits 32a and 32b, and then applied to the judgment circuit 20. In addition, S* associate calculation results means accumulated values of the frequency components until an S* code (a code inputted by this time).

The judgment circuit 20 shown in Figure 4 outputs a low level signal in judging that the square weighting addition value of the S0 associate calculation results or the square weighting addition value of the S2 associate calculation results is small, and outputs a high level signal in judging that the square weighting addition value of the S1 associate calculation results or the square weighting addition value of the S3 associate calculation results is small.

With referring to Figure 7, the DC component calculation circuit 30a includes DC component extraction circuits 34a to 34d for the S0 code to the S3 code. A DC component of the S0 code applied from the precoder 14 is extracted by the DC component extraction circuit 34a, and the S1 code to the S3 code are generated on the basis of the S0 code and then the DC components of the codes S1 to S3 are extracted by the DC component extraction circuits 34b to 34d, respectively. The extracted DC components are held for one code period by hold circuits 36a to 36e, respectively, and thereafter, outputs of the hold circuits 36a and 36c are applied to a switch 38a, and outputs of the hold circuits 36b and 36d are applied to a switch 38b. The switches 38a and 38b are controlled by the judgment signal obtained by judging the square weighting addition value of the preceding or last code such that two kinds of DC components having a chain relationship out of the four kinds of DC components held can be selected. More specifically, the DC components of the S0 code and the S1 code are selected when the judgment signal is the low level, and the DC components of the S2 code and the S3 code are selected when the judgment signal is the high level.

The DC components outputted from the switches 38a and 38b are applied to addition circuits 40a and 40b, respectively, and added to accumulation result which is obtained till the last or preceding code is outputted from a switch 38c. Addition values by addition circuits 40a and 40b are then held by hold circuits 36e and 36f, and outputs of the hold circuits 36e and 36f are applied to the square weighting addition circuits 32a and 32b as the calculation results, and to the switch 38c. In addition, the switch 38c is controlled by the judgment signal which judged the square weighting addition value of outputs of the hold circuits 36e and 36f, and selects the output of the hold circuit 36e when the judgment signal is the low level, and selects the output of the hold circuit 36f when the judgment signal is the high level. Therefore, the S0 associate calculation result and the S1 associate calculation circuit are outputted from the hold circuit 36e and 36f, respectively at a time that the judgment signal is the low level, and the S2 associate calculation result and the S3 associate calculation result are outputted from the hold circuits 36e and 36f, respectively when the judgment signal is the high level.

The switches 38a to 38c are thus changed-over, and therefore, the addition circuits 40a and 40b operate as a first addition means and a second addition means, a third addition means and a fourth addition means, a fifth addition means and a sixth addition means or a seventh addition means and a eighth addition means. Furthermore, the chain relationship of the DC components outputted from the switches 38a and 38b and the calculation results outputted from the hold circuits 36e and 36f are shown in Figure 12. More specifically, at a time that the DC components of code B0 to B3 are extracted by the DC component extraction circuits 34a to 34d, for example, if the judgment circuit 20 judges that a square weighting addition value of an A0 associate calculation result is the smallest in the square weighting addition values of the A0 associate calculation result and an A1 associate calculation result, the judgment signal of the low level is outputted from the judgment circuit 20. Therefore, the DC components of the B0 code and the B1 code are applied to the addition circuits 40a and 40b from the switches 38a and 38b, and the A0 associate calculation result is applied to the addition circuits 40a and 40b from the switch 38c.

Accordingly, the addition circuits 40a and 40b operate as the first addition means and the second addition means at this time. Therefore, a B0 associate calculation result (an addition value of the DC component of the B0 code and the A0 associate calculation result) and a B1 associate calculation result (an addition value of the DC component of the B1 code and the A0 associate calculation result) are outputted from the hold circuits 36e and 36f at a next time. Furthermore, at a time that the DC component of the C0 code to the C3 code of the succeeding input data c are extracted, if it is judged that the square weighting addition value of the B1 associate calculation result inputted to the judgment circuit 20 is small, the high level signal is outputted from the judgment circuit 20. Therefore, the DC components of the C2 code and C3 code are outputted from the switches 38a and 38b, and the B1 associate calculation result is outputted from the switch 38c. Accordingly, the addition circuits 40a and 40b operate as the third addition means and the fourth addition means at this time. Therefore, a C2 associate calculation result and a C3 associate calculation result are outputted from the hold circuits 36e and 36f at a next time.

Because of such a chain relation, the addition circuits 40a and 40b operate as the first addition means and the second addition means or the third addition means and the fourth addition means after they operated as the first addition means and the second addition means, and operate as the fifth addition means and the sixth addition means or the seventh addition means and the eighth addition means after they operated as the third addition means and the fourth addition means. Furthermore, the addition circuits 40a and 40b operate as the first addition means and the second addition means or the third addition means and the fourth addition means after the operation thereof as the fifth addition means and the sixth addition means, and operate as the fifth addition means and the sixth addition means or the seventh addition means and the eight addition means after the operation thereof as the seventh addition means and the eighth addition means.

In addition, though the frequency f1 sine component calculation circuit 30b, the frequency f1 cosine component calculation circuit 30c, the frequency f2 sine component calculation circuit 30d and the frequency f2 cosine component calculation circuit 30e are shown in Figure 8 to Figure 11, constitution of each of the calculation circuits 30b to 30e are the same as the DC component calculation circuit 30a except that the DC component extraction circuits 34a to 34e shown in Figure 7 are replaced with frequency f1 sine component extraction circuits 41a to 41d, frequency f1 cosine component extraction circuits 42a to 42d, frequency f2 sine component extraction circuits 44a to 44d and frequency f2 cosine component extraction circuits 46a to 46d, accordingly, duplicate description is omitted by adding the same referring numerals for the same point, and therefore by applying the same or similar reference numerals to the same or similar circuits, a duplicate description will be omitted here.

Constitution of the square weighting addition circuit 32a is shown in Figure 13. The S0 associate calculation results or the S2 associate calculation results outputted from the DC component calculation circuit 30a, the frequency f1 sine component calculation circuit 30b, the frequency f1 cosine component calculation circuit 30c, the frequency f2 sine component calculation circuit 30d and the frequency f2 cosine component calculation circuit 30e are squared by square circuits 48a to 48e, respectively. Then, though an output from the square circuit 48a is just weighted with predetermined value by a multiplication circuit 50a, outputs of the square circuits 48b and 48c are added to each other by an addition circuit 52a, and then, weighted by a multiplication circuit 50b, and outputs of square circuits 48d and 48e are also added to each other by an addition circuit 52b, and then, weighted by a multiplication circuit 50c. Thereafter, outputs of the multiplication circuits 50a to 50c are added to each other by an addition circuit 52c and then outputted to the judgment circuit 20. In addition, since a square weighting addition circuit 30b is constituted in the same manner as the square weighting addition circuit 32a, a duplicate description is omitted. However, the S1 associate calculation results or the S3 associate calculation results outputted from the DC component calculation circuit 30a, the frequency f1 sine component calculation circuit 30b, the frequency f1 cosine component calculation circuit 30c, the frequency f2 sine component calculation circuit 30d and the frequency f2 cosine component calculation circuit 30e are inputted to the square weighting addition circuit 32b.

Constitution of the 4-code generation circuit 22 of Figure 4 is shown in Figure 14. The S0 code via the delay circuit 16 is inputted to a switch 54 as it is, and applied to conversion circuits 56a to 56c to be converted to the S1 code, the

S2 code and the S3 code therein. The converted S1 code to the converted S3 code are then applied to the switch 54. Switch 54 is controlled by a selection switching circuit 58 which outputs a control signal on the basis of the inverted code signal, the last judgment signal and the present judgment signal, and selects and outputs one of the S0 code to the S3 code in accordance with a table 1.

Table 1

inverted cord signal	judgment signal		output
	present time	last time	
L	L	L	S0
	H	L	S1
	L	H	S2
	H	H	S3
H	L	-	S0
	H	-	S3

More specifically, in a case where the inverted code signal is a low level, the S0 code is outputted when both of the last judgment signal and the present judgment signal are the low levels, and the S1 code is outputted when the last judgment signal and the present judgment signal are the low level and the high level, respectively, and the S2 code is outputted when the present judgment signal and the present judgment signal are the high level and the low level, respectively, and the S3 code is outputted when both of the last judgment signal and the present judgment signal are the high level. Furthermore, in a case where the inverted code signal is a high level, the S0 code is outputted when the present inverted signal is the low level, and the S3 code is outputted when the present inverted signal is the high level.

An operation timing at a time that data is inputted is shown in Figure 15. When outputting of the reference code A0 of the input data "a" from the precoder 14 to the frequency component extraction circuit 18 is finished, outputting of the reference code B0 of the input data "b" is started at a next time. Since the judgment signal is the low level in the beginning, the switches 38a and 38b are connected to the hold circuits 36a and 36b and the components of the A0 code and the A1 code are outputted from the switches 38a and 38b. The judgment result for the A associate codes is determined in 15 clocks later, and the switches 38a to 38c are switched in response to the result. If the high level signal is outputted because a value of the A1 associate calculation results is smaller as a result of the judgement of the square weighting addition values of the A associate calculation results, the components of the B2 code and the B3 code are added to each other out of the A1 associate calculation results and four kinds of component extraction results, and the square weighting addition values of the B2 associate calculation results and the B3 associate calculation results are applied to the judgment circuit 20. Furthermore, the reference code A0 inputted to the 4-code generation circuit 22 with being delayed by the delay circuit 16 for 40 clocks is converted into the A1 code by the last judgment signal of the low level and the present judgment signal of the high level, and then outputted.

If the judgment circuit 20 judges that the square weighting addition value of the B2 associate calculation results is small at 15th clock from a timing that the precoder 14 begins to output the reference code C0 of the input data "c", and then outputs the low level signal, the B2 associate calculation results and the components of the C0 code and the C1 code are added to each other, and the square weighting addition values of the C0 associate calculation results and the C1 associate calculation results are applied to the judgment circuit 20. Furthermore, the reference code B0 inputted to the 4-code generation circuit 22 is converted into the B2 code by the last judgment signal of the high level and the present judgment signal of the low level.

If the judgment circuit 20 outputs the low level signal because the judgment circuit 20 judges that the square weighting addition value of the C0 associate calculation results is smaller at 15th clock from a timing that the precoder 14 begins to output the reference code D0 of the input data "d", the C0 associate calculation results and the components of the D0 code and the D1 code are added to each other, and the square weighting addition values of the D0 associate calculation results and the D1 associate calculation results are applied to the judgment circuit 20. Furthermore, since both of the last judgment signal and the present judgment signal are the low levels, the 4-code generation circuit 22 outputs the reference code C0 as it is.

A processing operation of the particular data that two kinds of particular codes are determined irrespective of the last code and used for the synchronization signal area, the overwrite margin area and etc. will be described. All bits have the inverted relationship about the two kinds of the particular codes RUN-A and RUN-B formats of which are determined by a specification for the particular data, as shown in Figure 16. More specifically, if the particular code RUN-A is assumed as the reference code S0, the particular code RUN-B is the S3 code. When the particular data is applied to the precoder 14, the inverted code signal of the high level is applied to the switches 24a and 24b simultaneously, whereby the outputs of the latch circuits 26a and 26b are applied to the input terminals of the EXOR circuit 28a and 28b, respectively. Therefore, a code outputted from the precoder 14 becomes the reference code S0 (the particular code RUN-A) even if the outputs from the latch circuits 26a and 26b are any of "00", "01", "10" and "11", as shown in Figure 17(A) to Figure 17(D).

In the frequency component extraction circuit 18, it is possible to process the particular data in the same manner as that of the S0 code to the S3 code of the normal data by generating and processing the S0 code by the respective component extraction circuits 34a, 40a, 42a, 44a and 46a for the S0 code and by generating the S3 code by the respective component extraction circuits 34b, 40b, 42b, 44b and 46b for the S1 code and generating the S0 code by the respective component extraction circuits 34c, 40c, 42c, 44c and 46c for the S2 code, and by generating the S3 code by the respective component extraction circuits 34d, 40d, 42d, 44d and 46d for the S3 code. Furthermore, the switch 54 of the 4-code generation circuit 22 is switched in response to only the present judgment signal. More specifically, as shown in the table 1, the S0 code is outputted from the switch 54 when the present judgment signal is the low level, and the S3 code is outputted from the switch 54 when the judgment signal is the high level.

By outputting one of the S0 code to the S3 code from the 4-code generation circuit 22 in accordance with the judgment signal outputted from the judgment circuit 20 and recording on the magnetic tape 60, codes which generates a frequency spectrum as shown in Figure 19(A) are resultingly recorded into a track 60a of the magnetic tape 60 shown in Figure 18, codes which generates frequency spectrum shown in Figure 19(B) are resultingly recorded into tracks 60b and 60d, and codes which generates a frequency spectrum shown in Figure 19(C) are resultingly recorded into a track 60c.

According to this embodiment, as is different from the prior art that the last two bits of the output code on the basis of the last input data is fed-back, the last two bits of the last or preceding code obtained by the I-NRZ modulation by the precoder 14 are fed-back, and therefore, there is no time restriction in performing the extraction operation of the frequency component and the judgment operation. Accordingly, it is possible to easily encode the input data.

In the embodiment shown in Figure 4, in a case where the judgment circuit 20 judges that the square weighting addition value of the B1 associate calculation results is the smallest in the square weighting addition values of the B0 associate calculation results and the B1 associate calculation results shown in Figure 12, for example, the square weighting addition values of the C2 associate calculation results and the C3 associate calculation results are inputted into the judgment circuit 20 at a next time. However, in a case where the square weighting additions values of the B0 associate calculation results and the B1 associate calculation results are approximately the same value, and the square weighting addition values of the C1 associate calculation results is the smallest in the square weighting addition values of the C0 associate calculation results to the C3 associate calculation results, there is a possibility that a code outputted from the 4-code generation circuit 22 is not always an optimum code. A coding apparatus 10 of another embodiment shown in Figure 20 is to improve such a problem.

With referring to Figure 20, since the coding apparatus 10 this embodiment shown is the same as the coding apparatus 10 of the embodiment shown in Figure 4 except that a frequency component extraction circuit 61 is constituted as shown in Figure 21, and a delay circuit 62 is a 65 clocks delay circuit, and a judgment circuit 63 judges on the basis of four (4) inputs, a duplicate description will be omitted by applying the same reference numerals to the same or similar points.

The frequency component extraction circuit 61 is constituted as shown in Figure 21. That is, the S0 code outputted from the precoder 14 is applied to a DC component calculation circuit 64a, a frequency f1 sine component calculation circuit 64b, a frequency f1 cosine component calculation circuit 64c, a frequency f2 sine component calculation circuit 64d and a frequency f2 cosine component calculation circuit 64e. Then, predetermined calculation operations are performed according to the judgment signal from the judgment circuit 20, and the S0 associate calculation results to the S3 associate calculation results are outputted therefrom. In these results, the S0 associate calculation results are applied to a square weighting addition circuit 66a, and the S1 associate calculation results are applied to a square weighting addition circuit 66b, and the S2 associate calculation results are applied to a square weighting addition circuit 66c, and the S3 associate calculation results are applied to a square weighting addition circuit 66d. Thereafter, operation results by the square weighting addition circuits 66a to 66d are applied to the judgment circuit 20. In addition, since the square weighting addition circuits 66a to 66d have the same constitution as that of the square weighting addition circuit 32a shown in Figure 13, a duplicate description will be omitted.

With referring to Figure 22, the S0 code outputted from the precoder 14 is applied to DC component extraction circuits 68a to 68d. Then, though the DC component of the S0 code is extracted by the DC component extraction circuit 68a, in the DC component extraction circuit 68b, the S1 code is generated on the basis of the S0 code as inputted, and then the DC component of the S1 code is extracted. As is the same as the DC component extraction circuit 68b, in the DC component extraction circuits 68c and 68d, the S2 code and the S3 code are generated on the basis of the S0 code, and then the DC components of the S2 code and the S3 code are extracted. The DC components extracted by the DC component extraction circuits 68a to 68d are applied to hold circuits 70a to 70d, and the DC components equal to one code are held therein. Then, the DC components outputted from the hold circuits 70a to 70d are added to calculation results outputted from switches 74a and 74b in addition circuits 72a to 72d.

More specifically, the DC component of the S0 code and the calculation result from the switch 74a are added to each other in the addition circuit 72a, and the DC component of the S1 code and the calculation result from the switch 74a are added to each other in the addition circuit 72b, and the DC component of the S2 code and the calculation result from the switch 74b are added to each other in the addition circuit 72c, and the DC component of the S3 code and the calculation result from the switch 74b are added to each other in the addition circuit 72d. The addition values outputted from the addition circuits 72a to 72d are held by hold circuits 76a to 76d, respectively, and then outputted to square weighting addition circuits 66a to 66d as the calculation result at a next time, respectively. Furthermore, outputs of the hold circuits 76a and 76c are applied to the switch 74a, and outputs of the hold circuits 76b and 76d are applied to the switch 74b. The switches 74a and 74b are switched in accordance with the judgment signal from the judgment circuit 22, and the outputs of the hold circuits 76a and 76b are outputted from the switches 74a and 74b when the judgment signal is the low level, and the outputs of the hold circuits 76c and 76d are outputted when the judgment signal is the high level.

By changing-one the switching of the switches 74a and 74b in such a manner, the addition circuits 72a to 72d operate as the first addition means to the fourth addition means or the fifth addition means to the eighth addition means. Furthermore, the chain relationship of the calculation results outputted from the hold circuits 76a to 76d is shown in Figure 12. That is, if the judgment signal is the high level, because the B0 associate calculation results to the B3 associate calculation results are outputted from the hold circuits 76a to 76d and the square weighting addition value thereof are judged by the judgment circuit 20, for example, the switches 74a and 74b are switched for the hold circuits 76c and 76d, respectively. Therefore, the B2 associate calculation results and the B3 associate calculation results outputted from the switches 74a and 74b are properly added to the DC components of the C0 code to the C3 code outputted from the hold circuits 70a to 70d. Accordingly, the addition circuits 72a to 72d operate as the fifth addition means to the eighth addition means at this time. Then, the C0 associate calculation results to the C3 associate calculation results are outputted from the hold circuits 76a to 76d at the next time, respectively. Thereafter, if the judgment signal is the low level because the C0 associate calculation results to the C3 associate calculation results are judged in the same manner, the C0 associate calculation results and the C1 associate calculation results outputted from the switches 74a to 74b are properly added to the DC components of the D0 code to the D3 code. Accordingly, the addition circuits 72a to 72b operate as the first addition means to the fourth addition means at this time. In addition, the judgment circuit 20 outputs the low level signal when the square weighting addition value of the S0 associate calculation results or the S1 associate calculation results is judged to be the smallest, and outputs the high level signal when the square weighting addition value of the S2 associate calculation results or the S3 associate calculation results is judged to be the smallest.

Because of such the chain relationship, the addition circuits 72a to 72d operate as the first addition means to the fourth addition means or the fifth addition means to the eighth addition means after the same operate as the first addition means to the fourth addition means, and operate as the first addition means to the fourth addition means or the fifth addition means to the eight addition means after the operation as the fifth addition means to the eight addition means.

With referring to Figure 23 to Figure 26, since the frequency f1 sine component calculation circuit 64b, the frequency f1 cosine component calculation circuit 64c, the frequency f2 sine component calculation circuit 64d and the frequency f2 cosine component calculation circuit 64e are the same as the DC component calculation circuit 64a except that frequency f1 sine component extraction circuits 78a to 78d, frequency f1 cosine component extraction circuits 80a to 80d, frequency f2 sine component extraction circuits 82a to 82d and frequency f2 cosine component extraction circuits 84a to 84d are provided instead of the DC component extraction circuits 68a to 68d shown in Figure 22, a duplicated description will be omitted by applying the same reference numerals to the same or similar components.

An operation timing is shown in Figure 27. When the outputting of the reference code A0 of the input data "a" from the precoder 14 to the frequency component extraction circuit 61 is finished, at a next time, the outputting of the reference code B0 of the input data "b" from the precoder 14 is started. Respective components of the A0 code to the A3 code are outputted from the hold circuits 70a to 70d at the same timing as the start of the output, and then, the judgment result of the square weighting addition value of the A associate calculation results is evaluated at 15th clock. The judgment result has no sense in a case of the chain of two codes, and the judgment signal maintains the low level thereof. Therefore, the A0 associate calculation results and the A1 associate calculation results are selected by the switches 74a and 74b, and then, the A0 associate calculation results and the components of the B0 code and the B1 code are added to each other by the addition circuits 72a and 72b, and the A1 associate calculation results and the components of the B2 code and the B3 code are added to each other by the addition circuits 72c and 72d.

The judgment result of the square weighting addition value of the B associate calculation results is evaluated at 15th clock from the timing that the components of the B0 code to the B3 code are outputted from the hold circuits 70a to 70d, i.e. 15th clock from the timing that the precoder 14 begins to output the reference code C0. If the judgment signal of the high level is outputted at this time because the square weighting addition value of the B2 associate calculation results or the B3 associate calculation results is the smallest, the B2 associate calculation results and the B3 associate calculation results are selected by the switches 74a and 74b, respectively, and then properly added to the components of the C0 code to the C3 code outputted from the hold circuits 70a to 70d. Furthermore, the A1 code is selected by the 4-code generation circuit 22 in accordance with the present judgment signal of the high level and the last judgment signal of the low level, and then outputted, as understood from the table 1.

The judgment result of the square weighting addition value of the C associate calculation results is evaluated at 15th clock from the timing that the components of the C0 code to the C3 code are outputted from the hold circuits 70a to 70d, that is, 15th clock from the timing that the precoder 14 begins to output the reference code D0. When the judgment signal of the low level is outputted because the judgment circuit 20 judges that the square weighting addition value of the C0 associate calculation results or the C1 associate calculation results is the smallest, the C0 associate calculation results and the C1 associate calculation results are selected by the selection circuits 74a and 74b, and then subjected to the next addition operation. That is, the C0 associate calculation results and the components of the D0 code and the D1 code are added to each other, and the C1 associate calculation results and the component of the D2 code and the D3 code are added to each other. Furthermore, the B2 code is outputted in accordance with the present judgment signal of the low level and the last judgment signal of the high level.

According to the Figure 20 embodiment, since the value obtained through the calculation of the codes for the next input data and the square weighting addition is judged, and the most suitable code of the data inputted before is to be outputted, it is possible to improve the problem occurs in the coding apparatus 10 shown in Figure 4. More specifically, in a case where the square weighting addition values of the B0 associate calculation results and the B1 associate calculation results shown in Figure 12 are almost the same value, and where the square weighting addition values of the C1 associate calculation results is the smallest in the square weighting addition values of the C0 associate calculation results to the C3 associate calculation results, since the operations for extracting the frequency components are executed with being made in chain with the B0 associate calculation results, the most suitable code is outputted from the 4-code generation circuit 22.

In addition, in order to further improve the problem included in the coding apparatus 10 shown in Figure 4, the number of the codes in chain may be increased. In such a case, it is necessary to provide 2^M of addition circuits and hold circuits at the next stage included in the frequency component calculation circuits and to provide 2^{M-1} of switches, according to the number M of the codes in chain, and to operate the first addition circuit to the 2^Mth addition circuit such that the calculation results of the frequency components can be outputted in a chain relationship shown in Figure 12.

Furthermore, in the above described embodiment, a code obtained by inserting "0" into the control bit and then by modulating the inserted data is regarded as the reference code, and three codes generated on the basis the reference code are regarded as the associate codes. However, it is clearly understood that the same operation becomes possible even if any one of the four kinds of codes is regarded as the reference code. Even more, the number of the bits of the code is not restricted to 25 bits.

Furthermore, though these embodiments are described with using the precoder 14 of a parallel system, the present invention is not restricted to this case, and it is clearly understood that the present invention can be applied to a case that a precoder of a serial system is used.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of restriction, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A coding method, comprising steps of:

   (a) inserting a control bit into input data;
   (b) generating a reference code on the basis of the input data into which said control bit is inserted;
   (c) generating a predetermined number of associate codes in association with said reference code; and
   (d) selectively outputting one of said reference code and said associate codes on the basis of frequency components of said reference code and said associate codes.

2. A coding method according to claim 1, wherein said step (d) includes steps of (d-1) extracting said frequency components of said reference code and said associate codes, (d-2) outputting a judgment signal on the basis of said frequency components, and (d-3) selecting one of said reference code and said associate codes in accordance with said judgment signal.

3. A coding apparatus, comprising:

   insertion means (12) for inserting a control bit into input data;

reference code generation means (14) for generating a reference code through I-NRZ modulation of data outputted from said insertion means;
associate code generation means (22, 56a, 56b, 56c) for generating a predetermined number of associate codes in association with said reference code on the basis of said reference code;
judgment signal outputting means (18, 20) for outputting a judgment signal on the basis of said frequency components of said reference code and said associate codes; and
code outputting means (22, 54) for selectively outputting one of said reference code and said associate codes in accordance with said judgment signal.

4. A coding apparatus according to claim 2, wherein said judgment means includes frequency component extracting means (18) for extracting a plurality of frequency components of said reference code and said plurality of codes associated with said reference code, and judgment means (20) for outputting said judgment signal by comparing said plurality of frequency components.

5. A coding apparatus according to claim 4, wherein said frequency component extraction means includes

first to Nth extraction means for extracting first to Nth (N is an integer) frequency components of each of said reference code and said associate codes,
first to Nth calculation means for calculating each of said first to Nth frequency components and outputting first to 2^Mth (M is a position integer) calculation results, and
first to 2^Mth operation means for operating each of said first to 2^Mth calculation results outputted from said first to Nth calculation means.

6. A coding apparatus according to claim 5, wherein each of said first to Nth extraction means includes frequency component extraction means for generating a first code, a second code and a third code on the basis of said reference code and extracting predetermined frequency components of said reference code, said first code, said second code and said third code.

7. A coding apparatus according to claim 6, each of said first to Nth calculation means includes

first addition means for adding said frequency components of said reference code at a present time and said calculation results of said frequency components of said reference code at a last time, thereby to regard addition results as said calculation results of said first frequency component of said reference code at said present time,
second addition means for adding said frequency components of said first code at said present time and said calculation results of said frequency components of said reference code at said last time, thereby to regard addition results as said calculation results of said first frequency component at said first code at said present time,
third addition means for adding said frequency components of said second code at said present time and said calculation results of said frequency components of said first code at said last time, thereby to regard addition results as said calculation results of said first frequency component of said second codes at said present time,
fourth addition means for adding said frequency components of said third code at said present time and said calculation results of said frequency components of said first code at said last time, thereby to regard addition results as said calculation results of said first frequency component of said third code at said present time,
fifth addition means for adding said frequency components of said reference code at said present time and said calculation results of said frequency components of said second code at said last time, thereby to regard addition results as said calculation results of said second frequency component of said reference code at said present time,
sixth addition means for adding said frequency components of said first code at said present time and said calculation results of said frequency components of said second code at said present time, thereby to regard addition results as said calculation results of said second frequency component of said first code at said present time,
seventh addition means for adding said frequency components of said second code at said present time and said calculation results of said frequency components of said third code at said last time, thereby to regard addition results as said calculation results of said second frequency component of said second code at said present time, and
eighth addition means for adding said frequency components of said third code at said present time and said calculation results of said frequency components of said third code at said last time, thereby to regard addition results as said calculation results of said second frequency component of said third code at said present time.

8. A coding apparatus according to claim 7, wherein each of said firs to Nth calculation means includes first and second adders for outputting said first and second calculation results, first setting means for operating said first adder as said first, third, fifth and seventh addition means, and second setting means for operating said second adder as said second, fourth, sixth and eighth addition means, in a case where M = 1.

9. A coding apparatus according to claim 7, wherein each of said first to Nth calculation means includes first to fourth adders for outputting said first to fourth calculation results, first setting means for operating said first adder as said first and fifth addition means, second setting means for operating said second adder as said second and sixth addition means, third setting means for operating said third adder as said third and seventh addition means, and fourth setting means for operating said fourth adder as said fourth and eighth addition means, in a case where M = 2.

10. A coding apparatus according to claim 7, wherein each of said first to Nth calculation means includes first to 2^Mth adders for outputting said first to 2^Mth calculation results, first setting means for operating (1 + 8n : n = 0, 1, 2, ..., 2^{M-3})th adder as first addition means, second setting means for operating (2 + 8n)th adder as second addition means, third setting means for operating (3 + 8n)th adder as third addition means, fourth setting means for operating (4 + 8n)th adder as fourth addition means, fifth setting means for operating (5 + 8n)th adder as fifth addition means, sixth setting means for operating (6 + 8n)th adder as sixth addition means, seventh setting means for operating (7 + 8n)th adder as seventh addition means, eighth setting means for operating (8 +8n)th adder as eight addition means, in a case where M ≧ 3.

11. A coding apparatus according to any of claims 3 to 10, wherein said reference code generation means includes replacing means (24a, 24b) for inserting predetermined one bit of said reference code at said last time instead of said control bit and for inserting predetermined one bit of said reference code at said last time instead of a first bit of said input data.

F I G. 1

(A)

MSB (INSERTION BIT) ↓

INPUT DATA a : $\underline{0}$ 1 0 1 1 0 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1

MODULATION SIGNAL $\underline{0\ 0}$ 0 1 0 0 1 0 1 0 0 1 0 0 0 1 1 1 1 0 0 1 1 1 1

CORD A 0 : 0 1 0 0 1 0 1 0 0 1 0 0 0 1 1 1 1 0 0 1 1 1 1 $\underline{0\ 0}$

(B)

MSB (INSERTION BIT) ↓

INPUT DATA a : $\underline{1}$ 1 0 1 1 0 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1

MODULATION SIGNAL $\underline{0\ 0}$ 1 1 1 0 0 0 0 0 1 1 1 0 1 1 0 1 0 0 1 1 0 1 0

CORD A 1 : 1 1 1 0 0 0 0 0 1 1 1 0 1 1 0 1 0 0 1 1 0 1 0 $\underline{0\ 1}$

F I G. 2

(A)

INPUT DATA b	0 1 0 1 1 0 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1
MODULATION SIGNAL	0 0 0 1 0 0 1 0 1 0 0 1 0 0 0 1 1 1 1 0 0 1 1 1 1
CORD B 0	: 0 1 0 0 1 0 1 0 0 1 0 0 0 1 1 1 1 0 0 1 1 1 1 0 0

(B)

INPUT DATA b	1 1 0 1 1 0 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1
MODULATION SIGNAL	0 0 1 1 1 0 0 0 0 0 1 1 1 0 1 1 0 1 0 0 1 1 0 1 0
CORD B 1	: 1 1 1 0 0 0 0 0 1 1 1 0 1 1 0 1 0 0 1 1 0 1 0 0 1

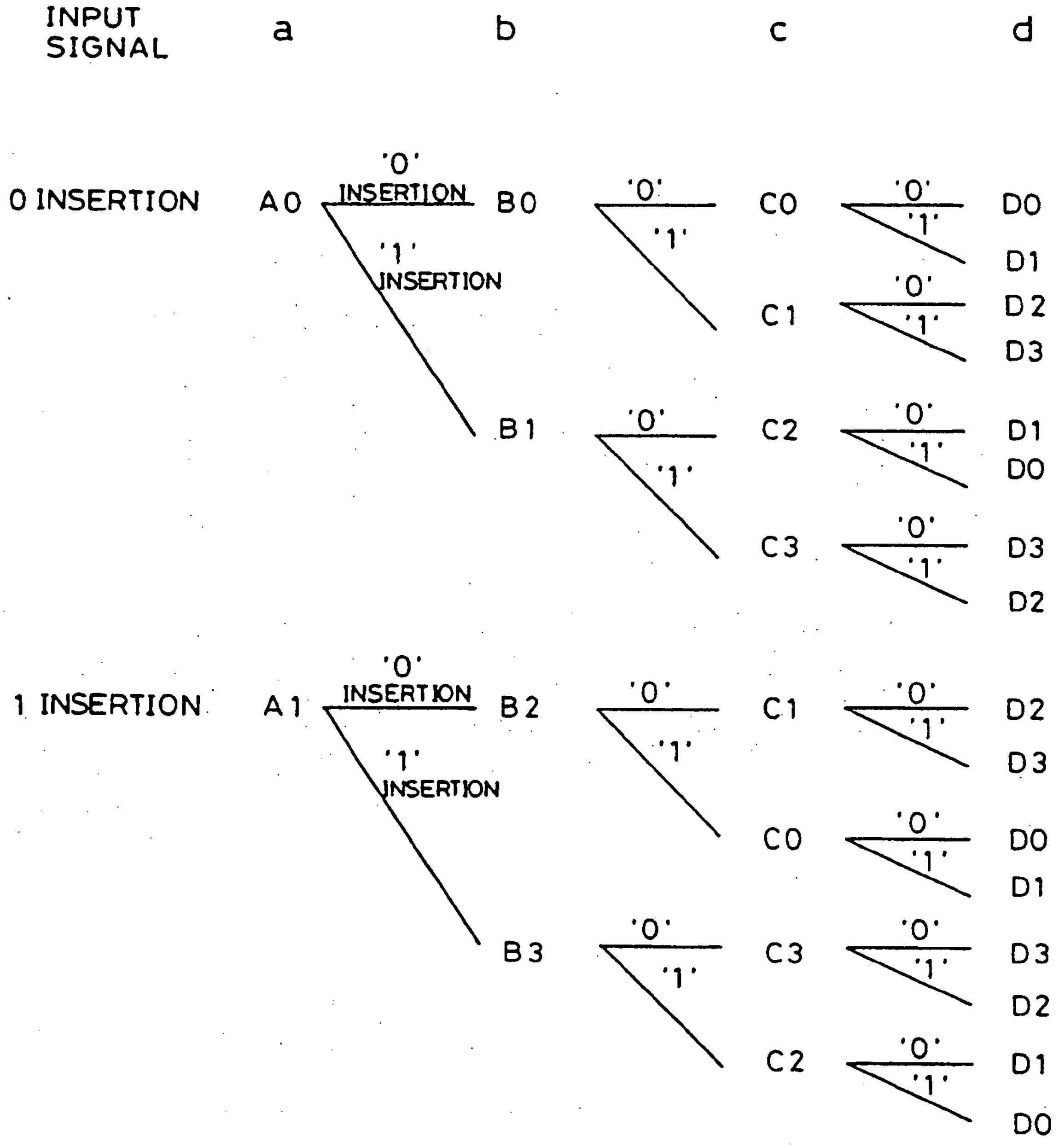
(C)

INPUT DATA b	0 1 0 1 1 0 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1
MODULATION SIGNAL	0 1 0 0 0 1 1 1 1 1 0 0 0 1 0 0 1 0 1 1 0 0 1 0 1
CORD B 2	: 0 0 0 1 1 1 1 1 0 0 0 1 0 0 1 0 1 1 0 0 1 0 1 1 0

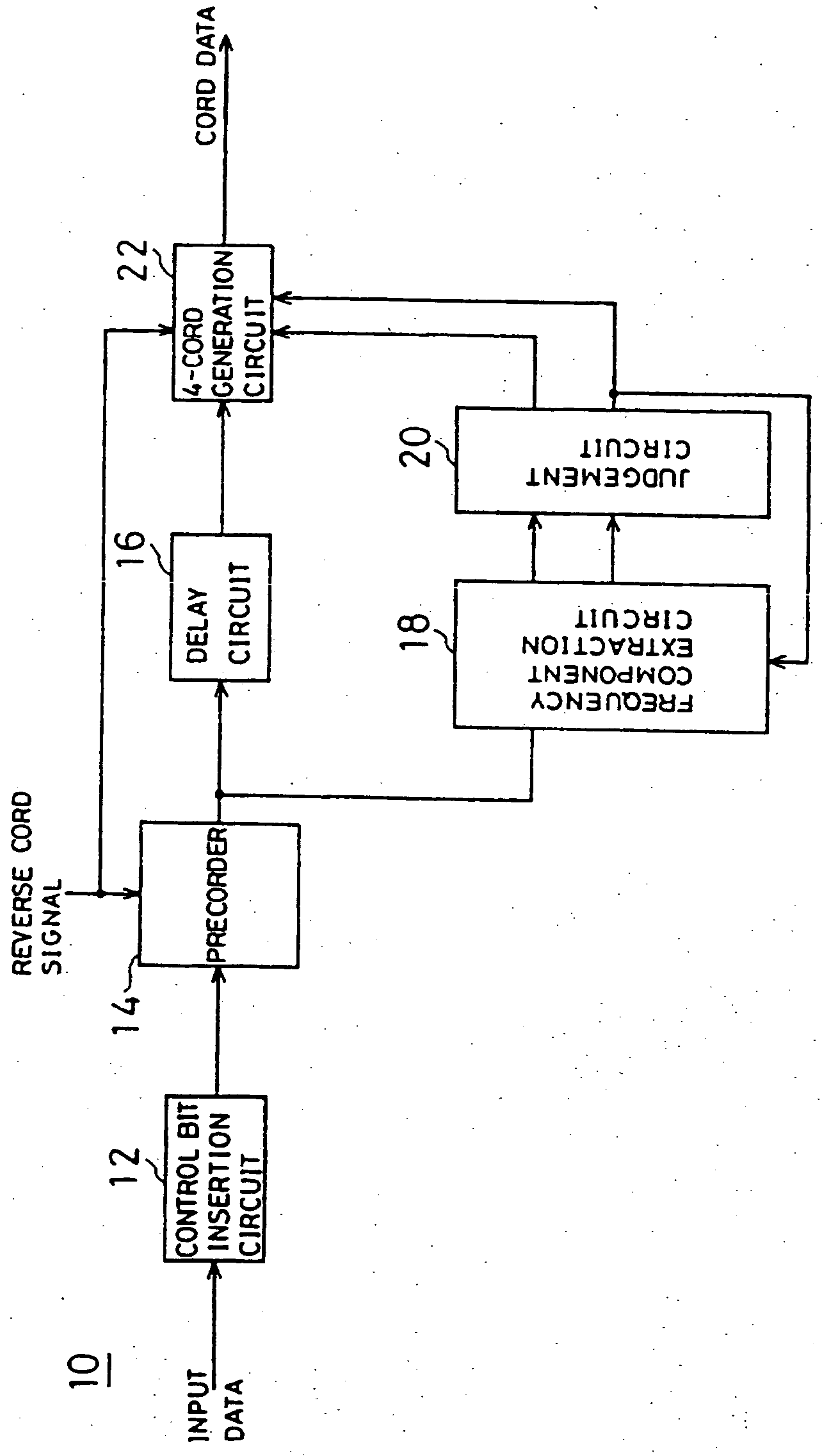
(D)

INPUT DATA b	1 1 0 1 1 0 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1
MODULATION SIGNAL	0 1 1 0 1 1 0 1 0 1 1 0 1 1 1 0 0 0 0 1 1 0 0 0 0
CORD B 3	: 1 0 1 1 0 1 0 1 1 0 1 1 1 0 0 0 0 1 1 0 0 0 0 1 1

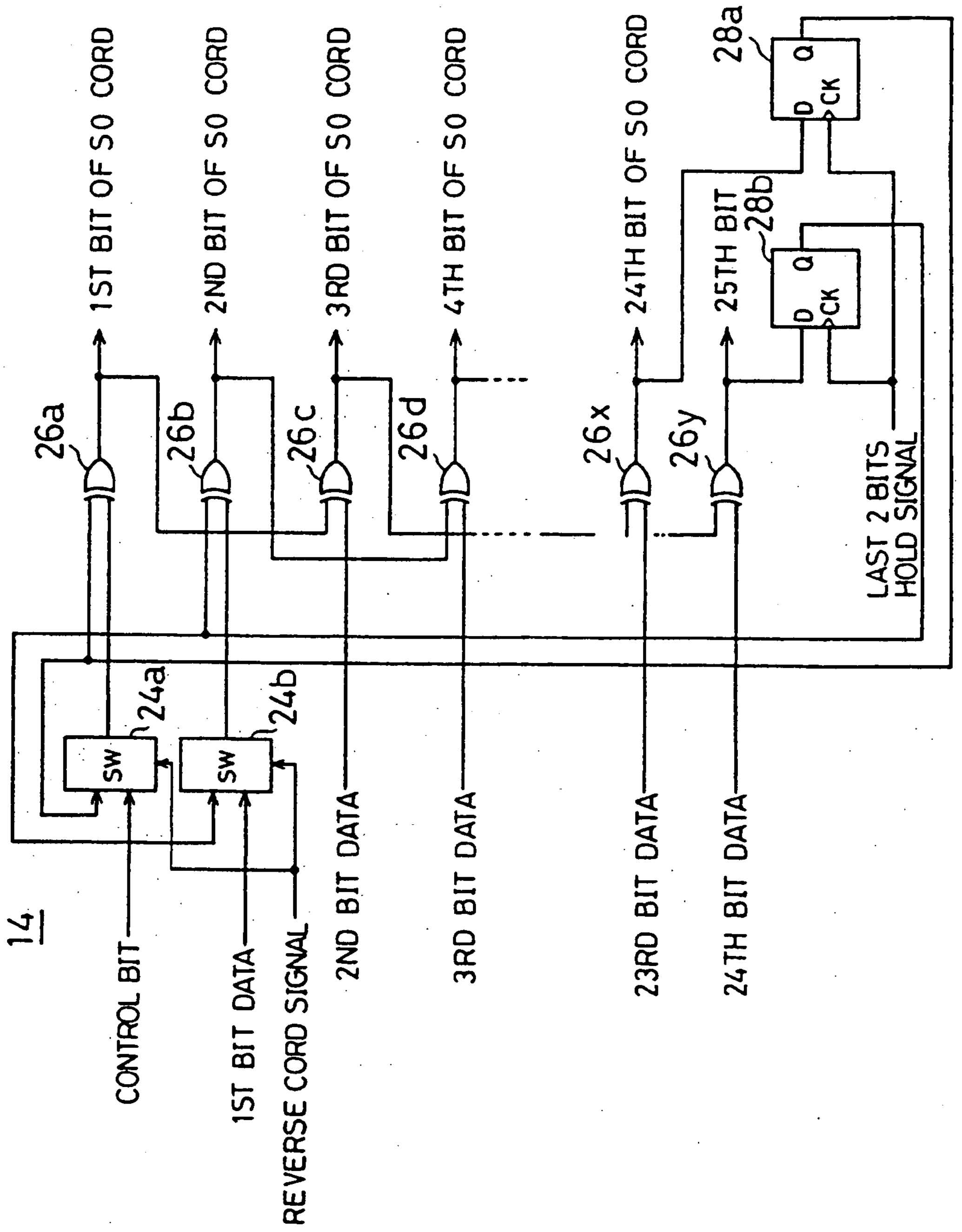
FIG. 3


INPUT SIGNAL
a
b
c
d
0 INSERTION
A0
'0' INSERTION
B0
'1' INSERTION
B1
'0'
'1'
C0
C1
C2
C3
D0
D1
D2
D3
D1
D0
D3
D2
1 INSERTION
A1
'0' INSERTION
B2
'1' INSERTION
B3
C1
C0
C3
C2
D2
D3
D0
D1
D3
D2
D1
D0

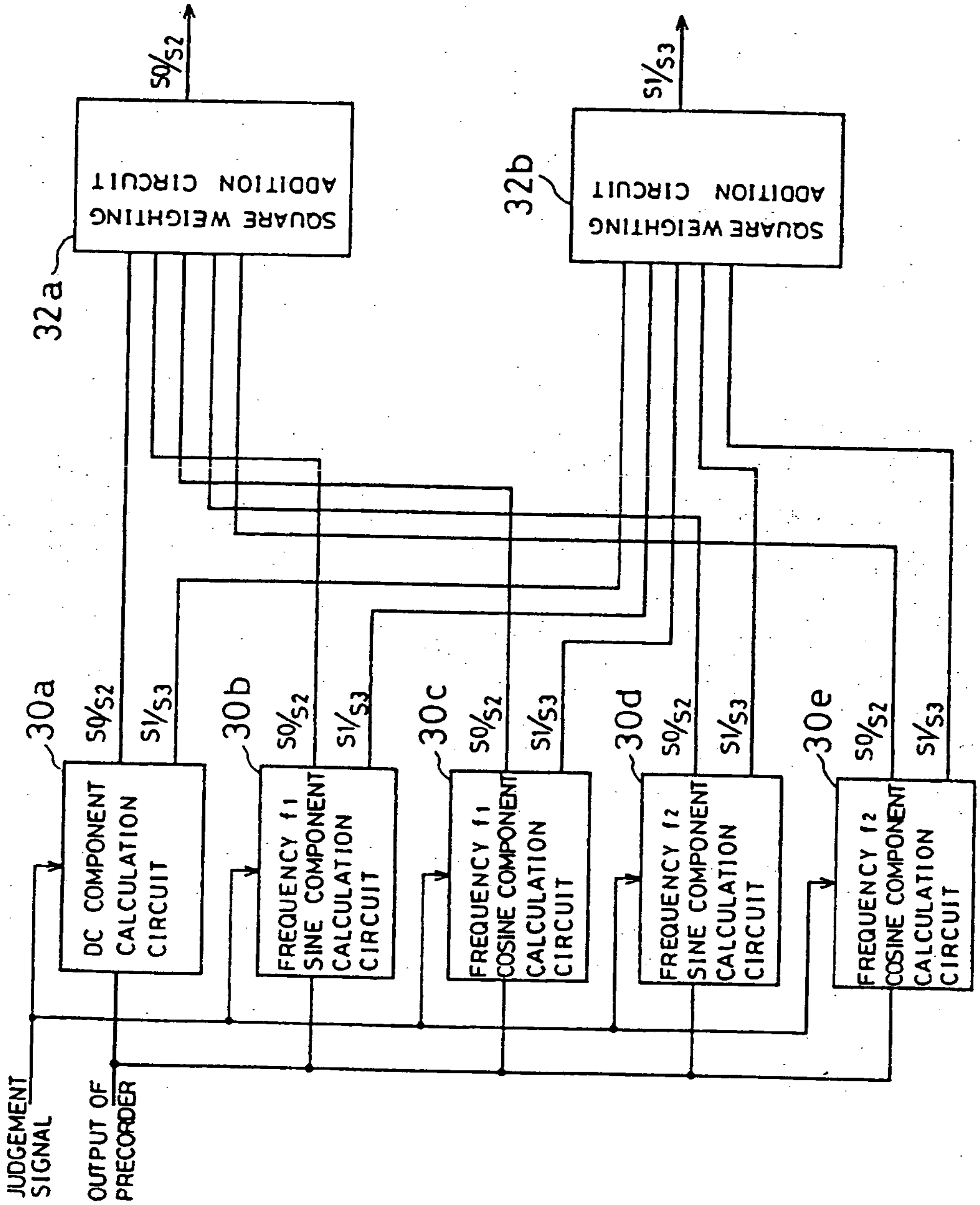
F I G. 4


10
INPUT DATA
CONTROL BIT INSERTION CIRCUIT
12
PRECORDER
14
REVERSE CORD SIGNAL
DELAY CIRCUIT
16
FREQUENCY COMPONENT EXTRACTION CIRCUIT
18
JUDGEMENT CIRCUIT
20
4-CORD GENERATION CIRCUIT
22
CORD DATA

F I G. 5


14
CONTROL BIT
1ST BIT DATA
REVERSE CORD SIGNAL
2ND BIT DATA
3RD BIT DATA
23RD BIT DATA
24TH BIT DATA
SW
SW
24a
24b
26a
26b
26c
26d
26x
26y
1ST BIT OF SO CORD
2ND BIT OF SO CORD
3RD BIT OF SO CORD
4TH BIT OF SO CORD
24TH BIT OF SO CORD
25TH BIT
28a
28b
D
CK
Q
D
CK
Q
LAST 2 BITS HOLD SIGNAL

F I G. 6


JUDGEMENT SIGNAL
OUTPUT OF PRECORDER
DC COMPONENT CALCULATION CIRCUIT
30a
S0/S2
S1/S3
FREQUENCY f1 SINE COMPONENT CALCULATION CIRCUIT
30b
S0/S2
S1/S3
FREQUENCY f1 COSINE COMPONENT CALCULATION CIRCUIT
30c
S0/S2
S1/S3
FREQUENCY f2 SINE COMPONENT CALCULATION CIRCUIT
30d
S0/S2
S1/S3
FREQUENCY f2 COSINE COMPONENT CALCULATION CIRCUIT
30e
S0/S2
S1/S3
SQUARE WEIGHTING ADDITION CIRCUIT
32a
S0/S2
SQUARE WEIGHTING ADDITION CIRCUIT
32b
S1/S3

F I G. 7

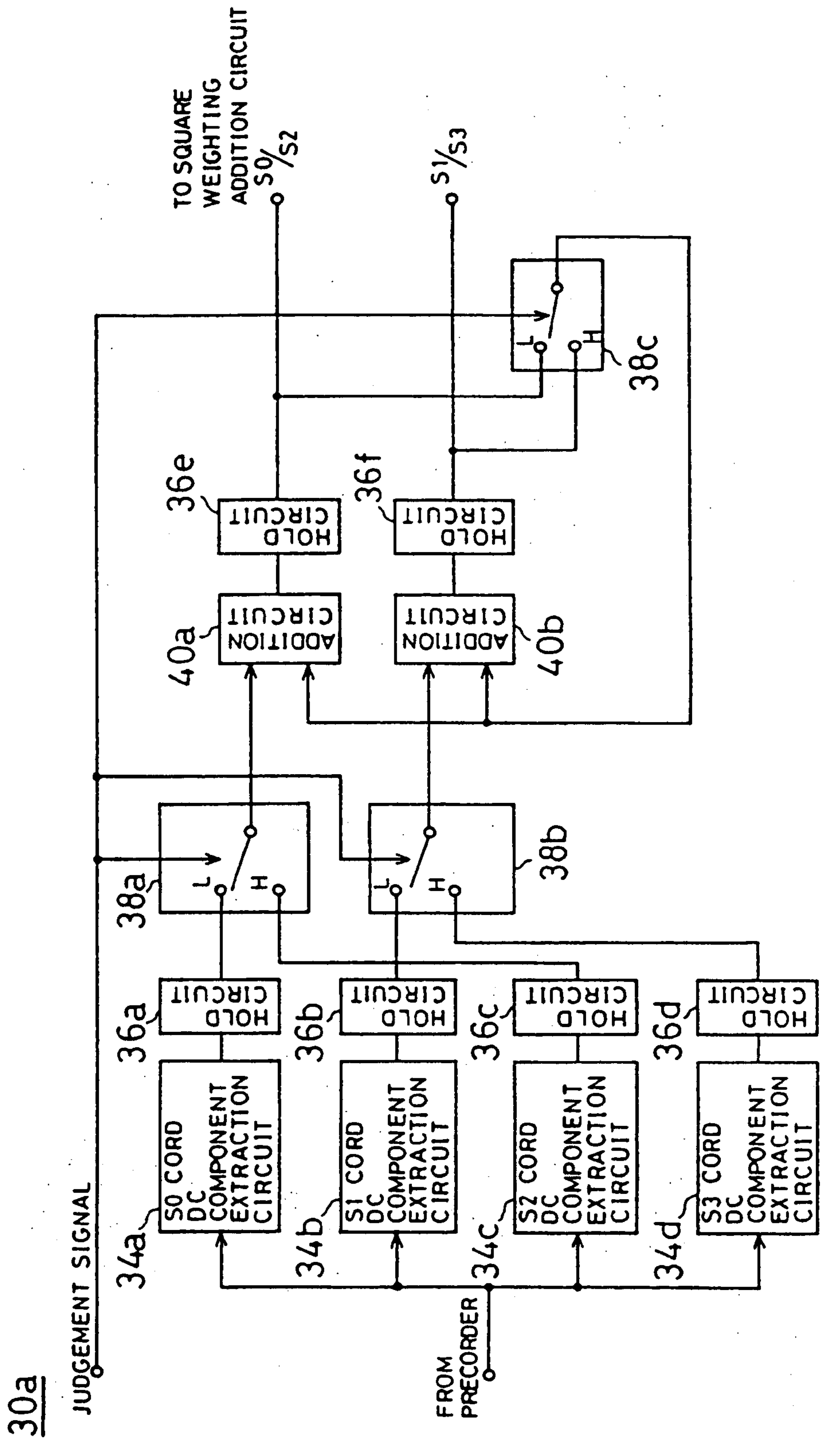

30a
JUDGEMENT SIGNAL
FROM PRECORDER
34a
S0 CORD DC COMPONENT EXTRACTION CIRCUIT
34b
S1 CORD DC COMPONENT EXTRACTION CIRCUIT
34c
S2 CORD DC COMPONENT EXTRACTION CIRCUIT
34d
S3 CORD DC COMPONENT EXTRACTION CIRCUIT
36a
HOLD CIRCUIT
36b
HOLD CIRCUIT
36c
HOLD CIRCUIT
36d
HOLD CIRCUIT
38a
L
H
38b
L
H
40a
ADDITION CIRCUIT
40b
ADDITION CIRCUIT
36e
HOLD CIRCUIT
36f
HOLD CIRCUIT
38c
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0/S2
S1/S3

FIG. 8

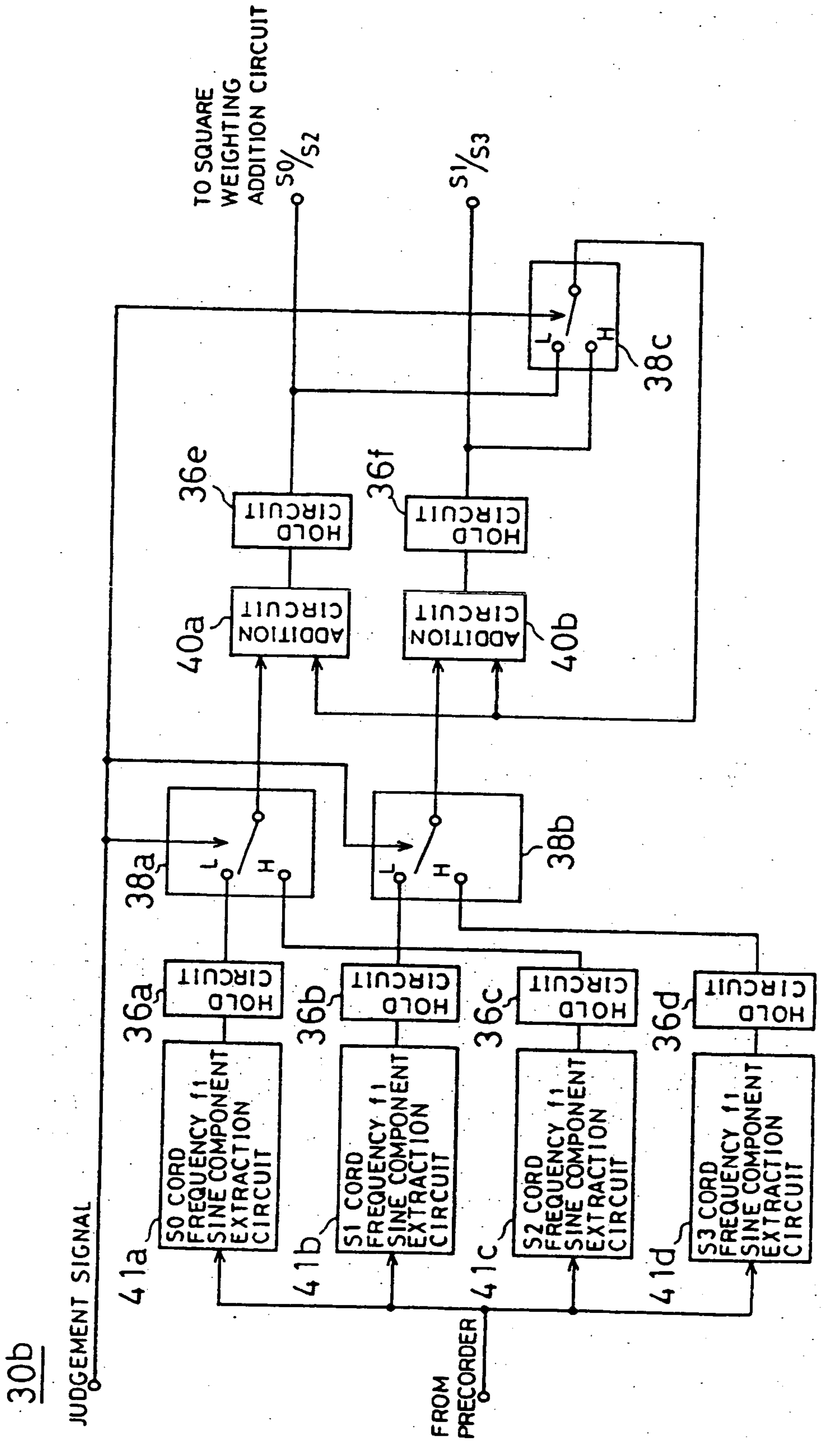

30b
JUDGEMENT SIGNAL
FROM PRECORDER
41a
S0 CORD FREQUENCY f1 SINE COMPONENT EXTRACTION CIRCUIT
41b
S1 CORD FREQUENCY f1 SINE COMPONENT EXTRACTION CIRCUIT
41c
S2 CORD FREQUENCY f1 SINE COMPONENT EXTRACTION CIRCUIT
41d
S3 CORD FREQUENCY f1 SINE COMPONENT EXTRACTION CIRCUIT
36a
HOLD CIRCUIT
36b
HOLD CIRCUIT
36c
HOLD CIRCUIT
36d
HOLD CIRCUIT
38a
L
H
38b
L
H
40a
ADDITION CIRCUIT
40b
ADDITION CIRCUIT
36e
HOLD CIRCUIT
36f
HOLD CIRCUIT
38c
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0/S2
S1/S3

FIG. 9

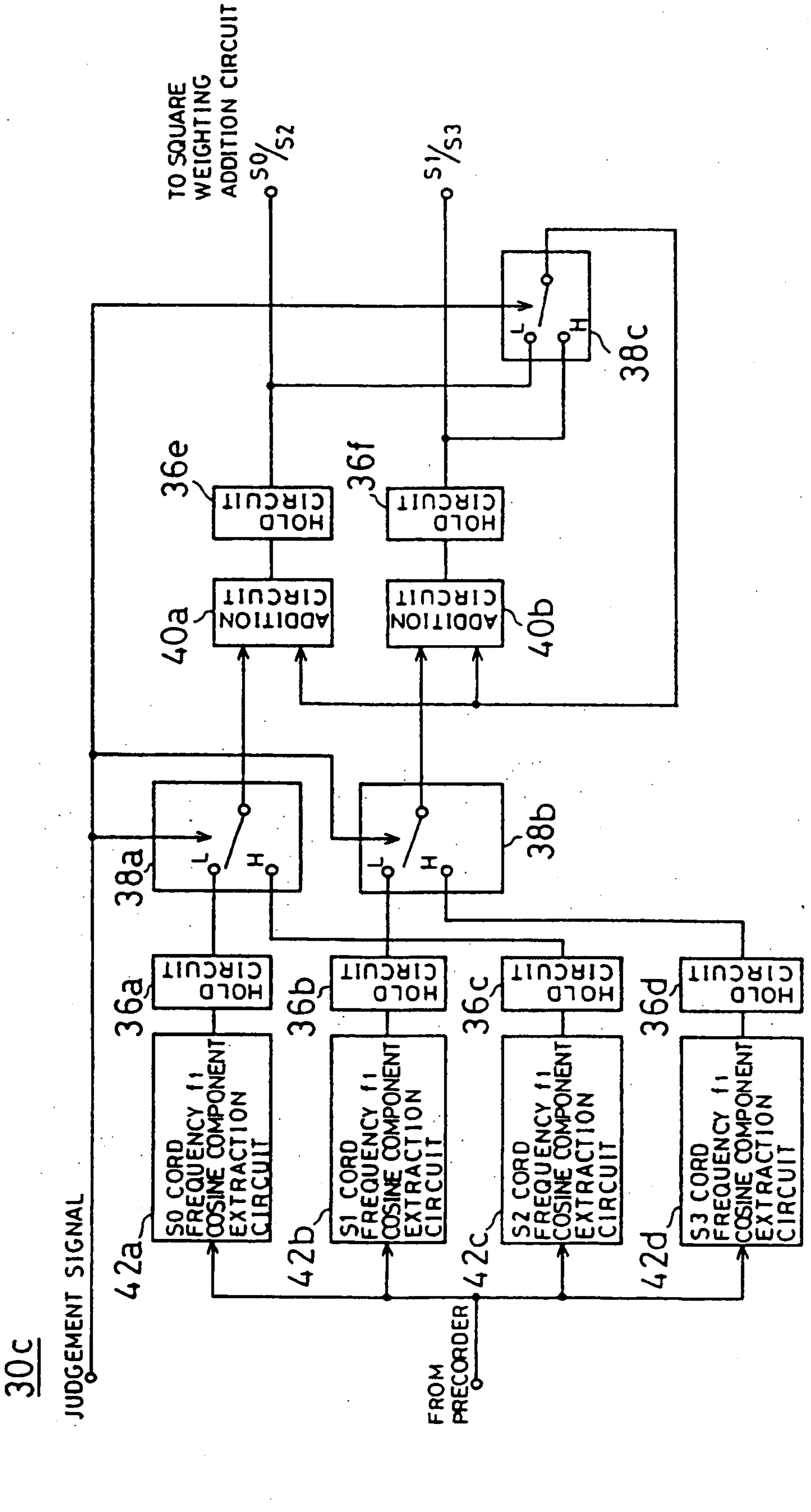
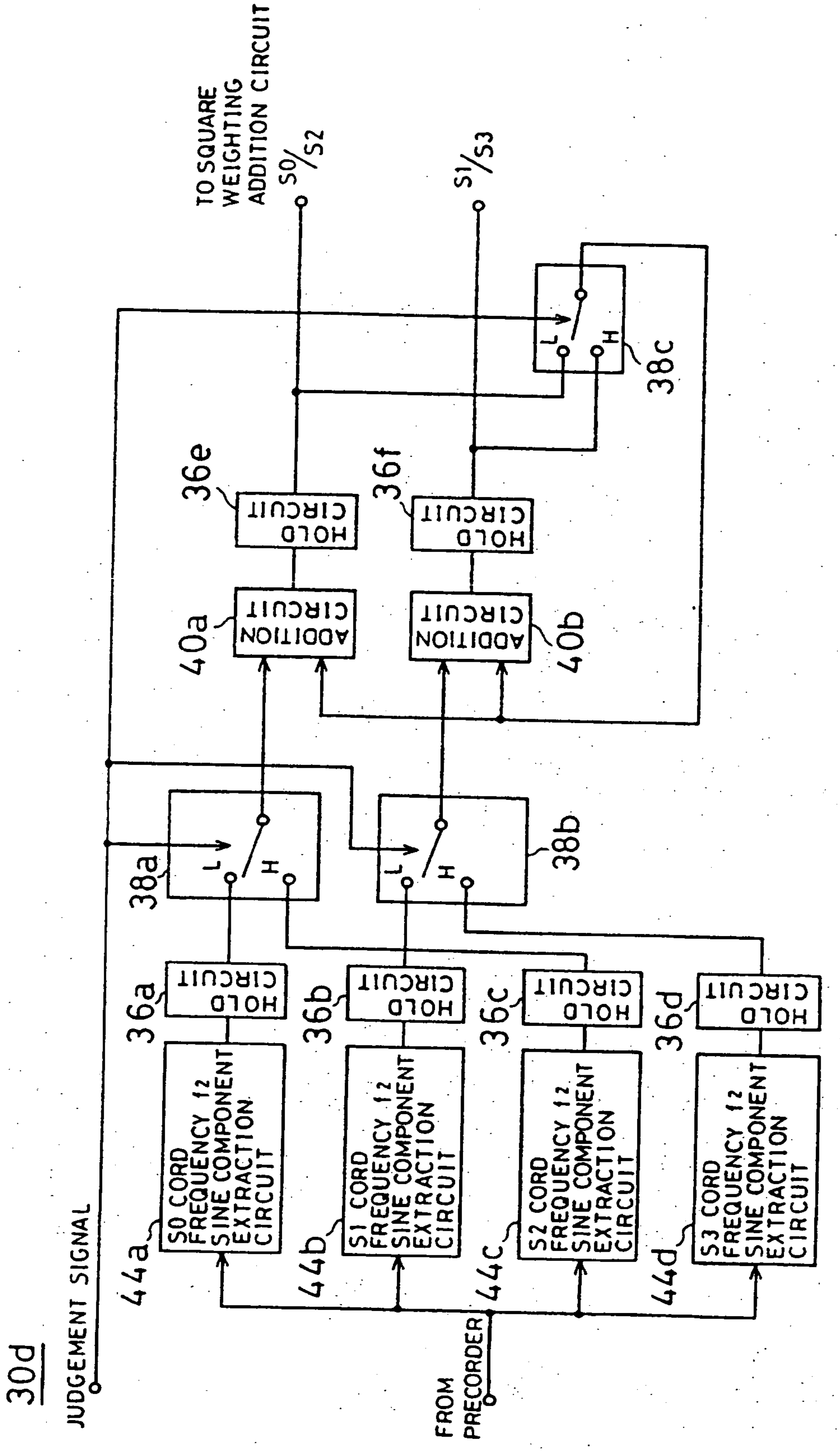
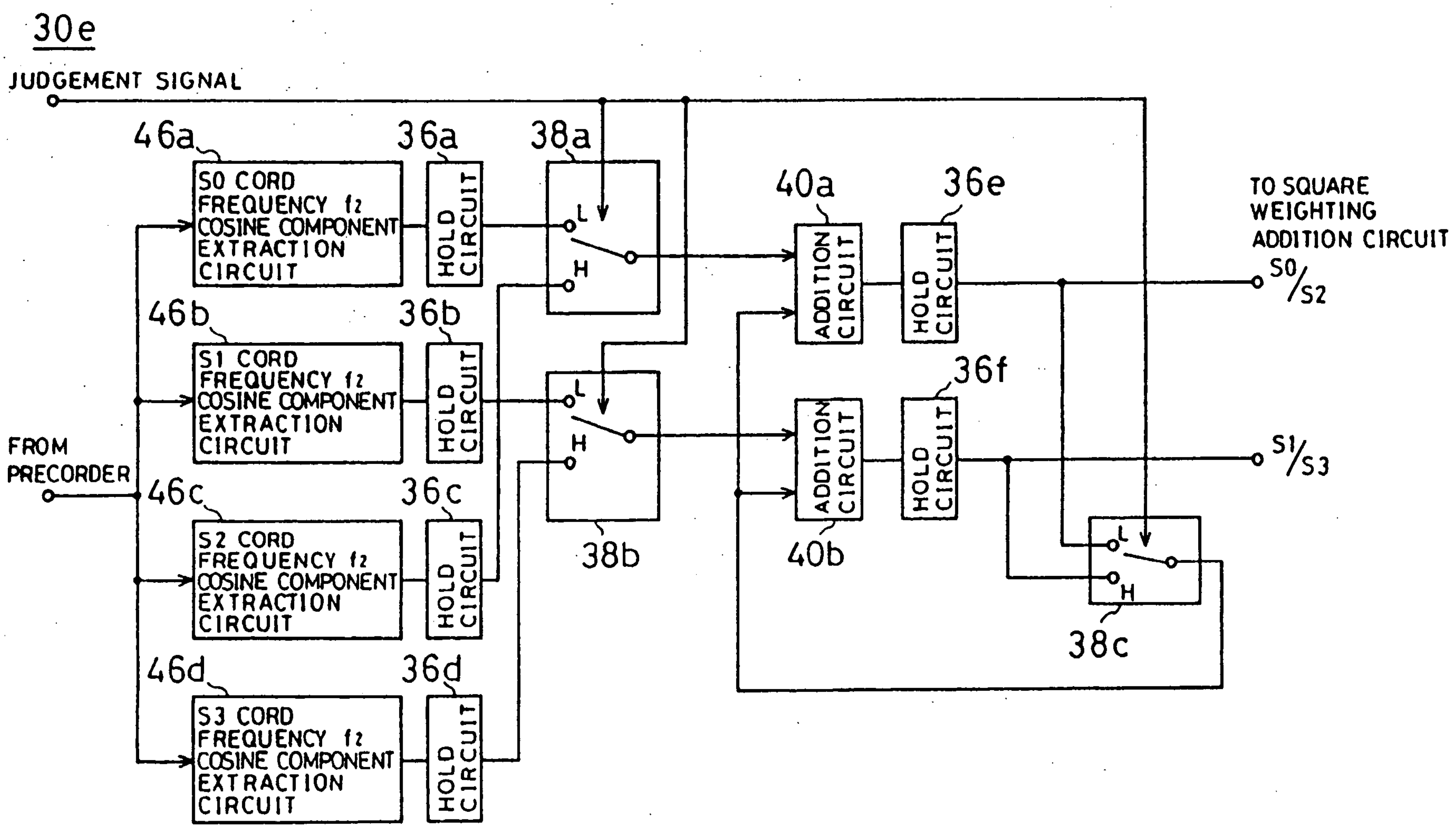

30c
JUDGEMENT SIGNAL
FROM PRECORDER
42a
S0 CORD FREQUENCY f1 COSINE COMPONENT EXTRACTION CIRCUIT
42b
S1 CORD FREQUENCY f1 COSINE COMPONENT EXTRACTION CIRCUIT
42c
S2 CORD FREQUENCY f1 COSINE COMPONENT EXTRACTION CIRCUIT
42d
S3 CORD FREQUENCY f1 COSINE COMPONENT EXTRACTION CIRCUIT
36a
HOLD CIRCUIT
36b
HOLD CIRCUIT
36c
HOLD CIRCUIT
36d
HOLD CIRCUIT
38a
L
H
38b
L
H
40a
ADDITION CIRCUIT
40b
ADDITION CIRCUIT
36e
HOLD CIRCUIT
36f
HOLD CIRCUIT
38c
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0/S2
S1/S3

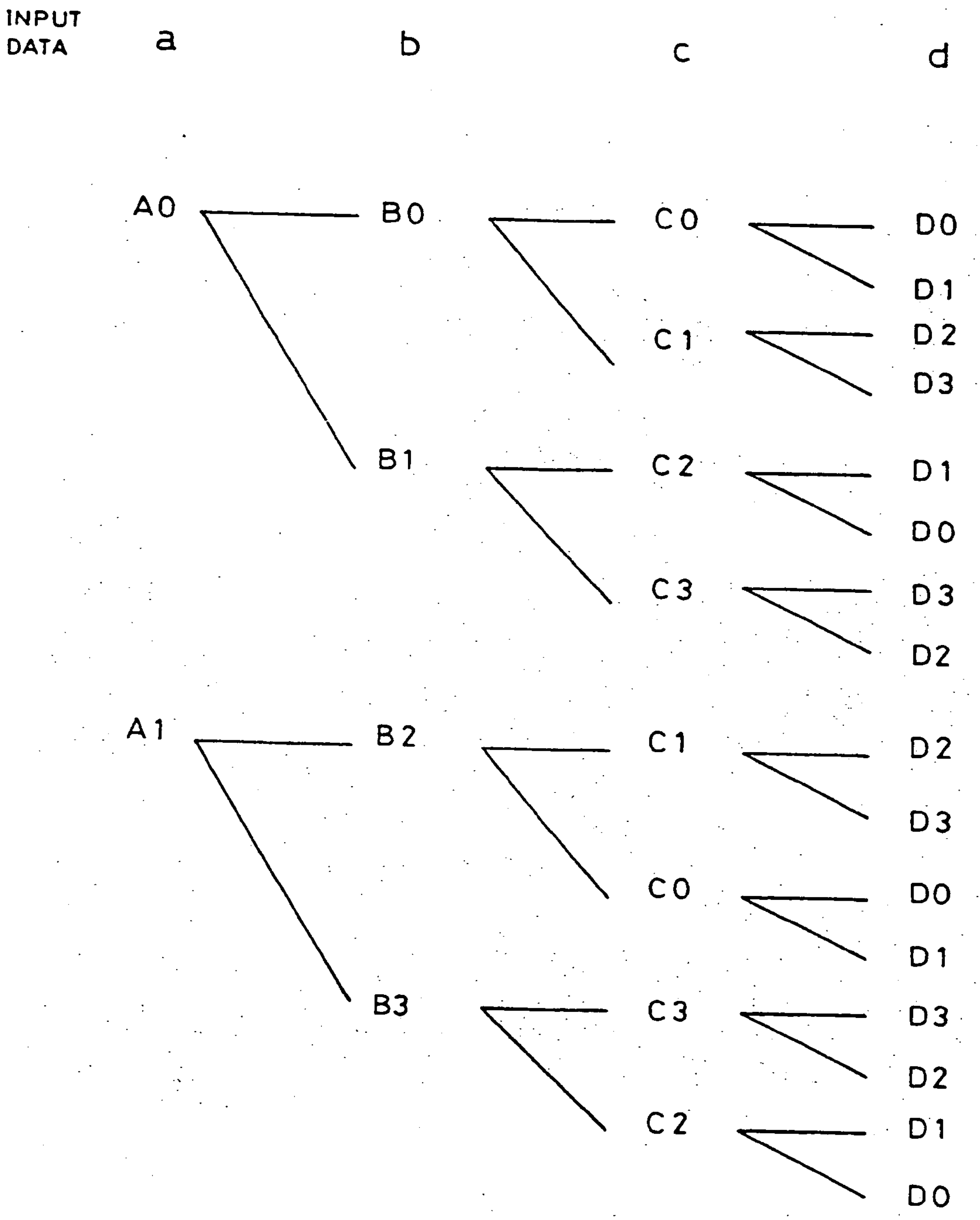
FIG. 10


30d
JUDGEMENT SIGNAL
FROM PRECORDER
44a
S0 CORD FREQUENCY f2 SINE COMPONENT EXTRACTION CIRCUIT
44b
S1 CORD FREQUENCY f2 SINE COMPONENT EXTRACTION CIRCUIT
44c
S2 CORD FREQUENCY f2 SINE COMPONENT EXTRACTION CIRCUIT
44d
S3 CORD FREQUENCY f2 SINE COMPONENT EXTRACTION CIRCUIT
36a
HOLD CIRCUIT
36b
HOLD CIRCUIT
36c
HOLD CIRCUIT
36d
HOLD CIRCUIT
38a
L
H
38b
L
H
40a
ADDITION CIRCUIT
40b
ADDITION CIRCUIT
36e
HOLD CIRCUIT
36f
HOLD CIRCUIT
38c
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0/S2
S1/S3

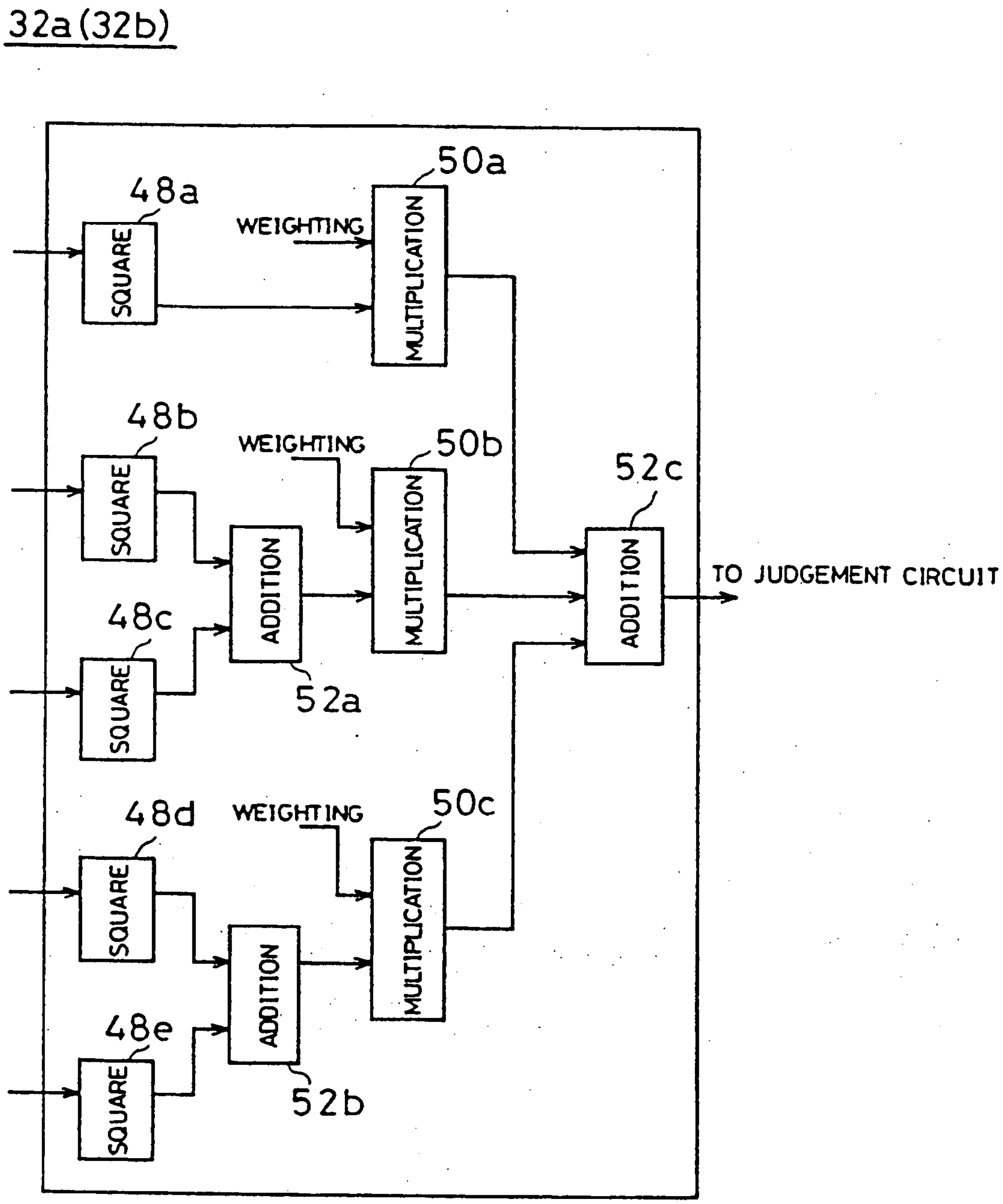
F I G. 11


30e
JUDGEMENT SIGNAL
FROM PRECORDER
46a
S0 CORD FREQUENCY f2 COSINE COMPONENT EXTRACTION CIRCUIT
46b
S1 CORD FREQUENCY f2 COSINE COMPONENT EXTRACTION CIRCUIT
46c
S2 CORD FREQUENCY f2 COSINE COMPONENT EXTRACTION CIRCUIT
46d
S3 CORD FREQUENCY f2 COSINE COMPONENT EXTRACTION CIRCUIT
36a
HOLD CIRCUIT
36b
HOLD CIRCUIT
36c
HOLD CIRCUIT
36d
HOLD CIRCUIT
38a
L
H
38b
L
H
40a
ADDITION CIRCUIT
40b
ADDITION CIRCUIT
36e
HOLD CIRCUIT
36f
HOLD CIRCUIT
38c
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0/S2
S1/S3

F I G.12


INPUT DATA
a
b
c
d
A0
B0
C0
D0
D1
C1
D2
D3
B1
C2
D1
D0
C3
D3
D2
A1
B2
C1
D2
D3
C0
D0
D1
B3
C3
D3
D2
C2
D1
D0

F I G. 13


32a (32b)
48a
SQUARE
WEIGHTING
50a
MULTIPLICATION
48b
SQUARE
WEIGHTING
50b
MULTIPLICATION
52c
ADDITION
TO JUDGEMENT CIRCUIT
48c
SQUARE
ADDITION
52a
48d
SQUARE
WEIGHTING
50c
MULTIPLICATION
ADDITION
48e
SQUARE
52b

F I G.14

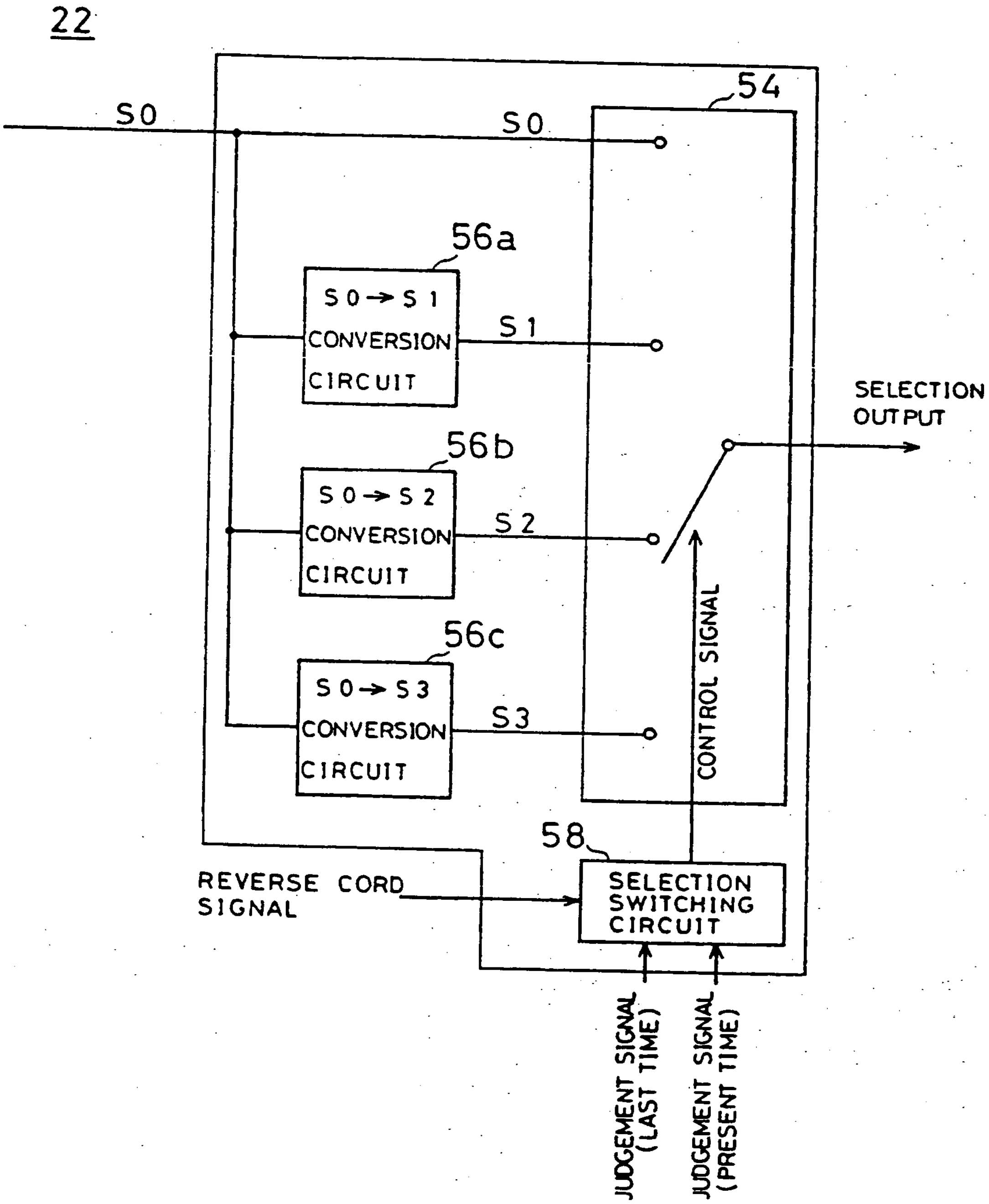

22
S0
S0
54
56a
S0→S1
CONVERSION
CIRCUIT
S1
SELECTION
OUTPUT
56b
S0→S2
CONVERSION
CIRCUIT
S2
CONTROL SIGNAL
56c
S0→S3
CONVERSION
CIRCUIT
S3
58
REVERSE CORD
SIGNAL
SELECTION
SWITCHING
CIRCUIT
JUDGEMENT SIGNAL
(LAST TIME)
JUDGEMENT SIGNAL
(PRESENT TIME)

FIG.15

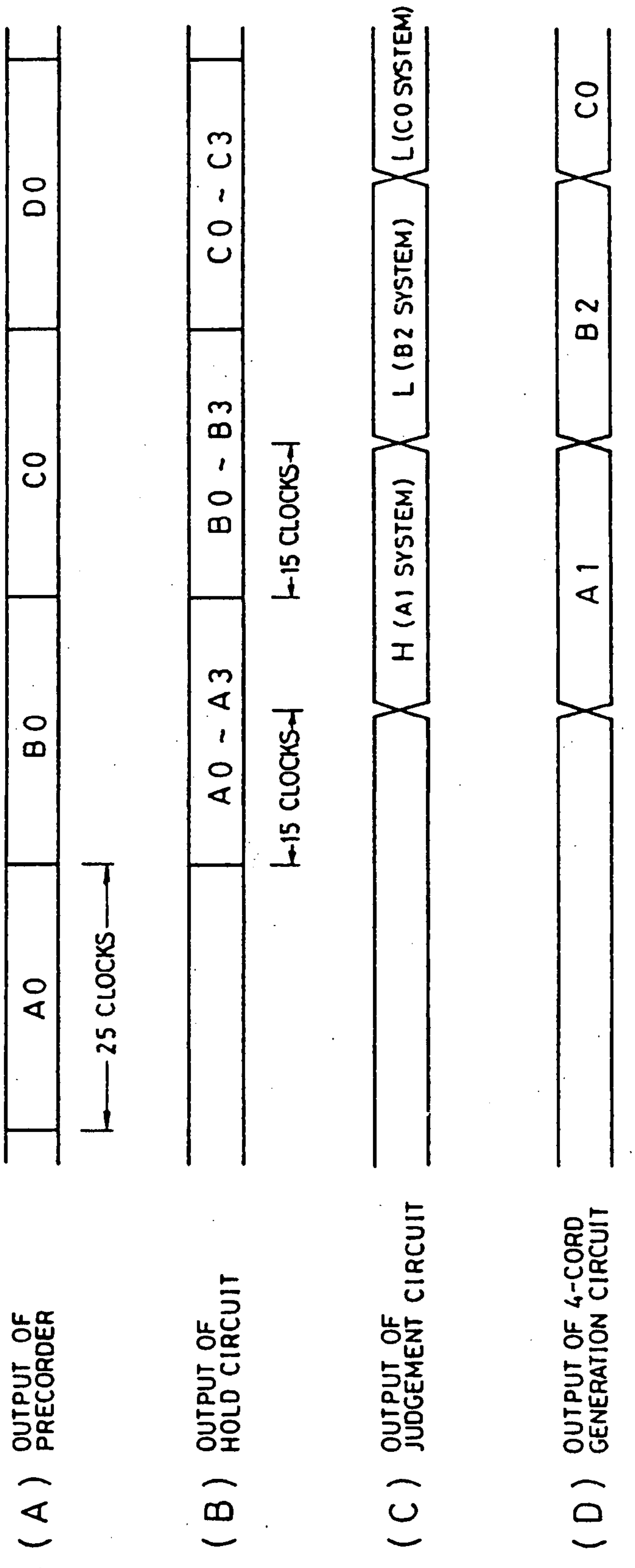

(A) OUTPUT OF PRECORDER
A0
B0
C0
D0
25 CLOCKS
(B) OUTPUT OF HOLD CIRCUIT
A0 ~ A3
B0 ~ B3
C0 ~ C3
15 CLOCKS
15 CLOCKS
(C) OUTPUT OF JUDGEMENT CIRCUIT
H (A1 SYSTEM)
L (B2 SYSTEM)
L (C0 SYSTEM)
(D) OUTPUT OF 4-CORD GENERATION CIRCUIT
A1
B2
C0

FIG.16

RUN-A : 0001110001110000011100011

RUN-B : 1110001110001111100011100

F I G. 17

(A)

INSERTED 2 BITS ↓

INPUT DATA 00 | 0 1 1 0 1 1 0 1 1 0 1 1 0 0 0 1 1 0 1 1 0 1 1

MODULATION SIGNAL 00 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0

REFERENCE CORD S0 (RUN-A) : 00 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0 1 1

(B)

INSERTED 2 BITS ↓

INPUT DATA 01 | 0 1 1 0 1 1 0 1 1 0 1 1 0 0 0 1 1 0 1 1 0 1 1

MODULATION SIGNAL 01 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0

REFERENCE CORD S0 (RUN-A) : 00 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0 1 1

(C)

INSERTED 2 BITS ↓

INPUT DATA 10 | 0 1 1 0 1 1 0 1 1 0 1 1 0 0 0 1 1 0 1 1 0 1 1

MODULATION SIGNAL 10 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0

REFERENCE CORD S0 (RUN-A) : 00 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0 1 1

(D)

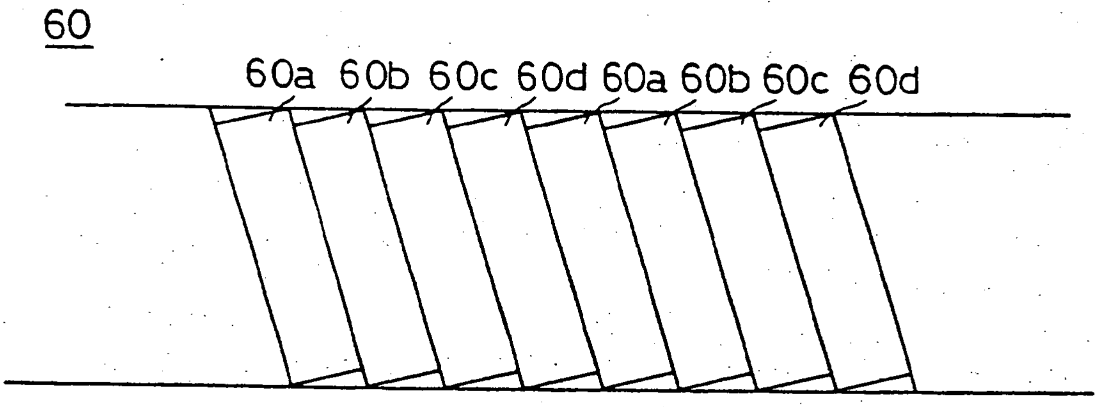
INSERTED 2 BITS ↓

INPUT DATA 11 | 0 1 1 0 1 1 0 1 1 0 1 1 0 0 0 1 1 0 1 1 0 1 1

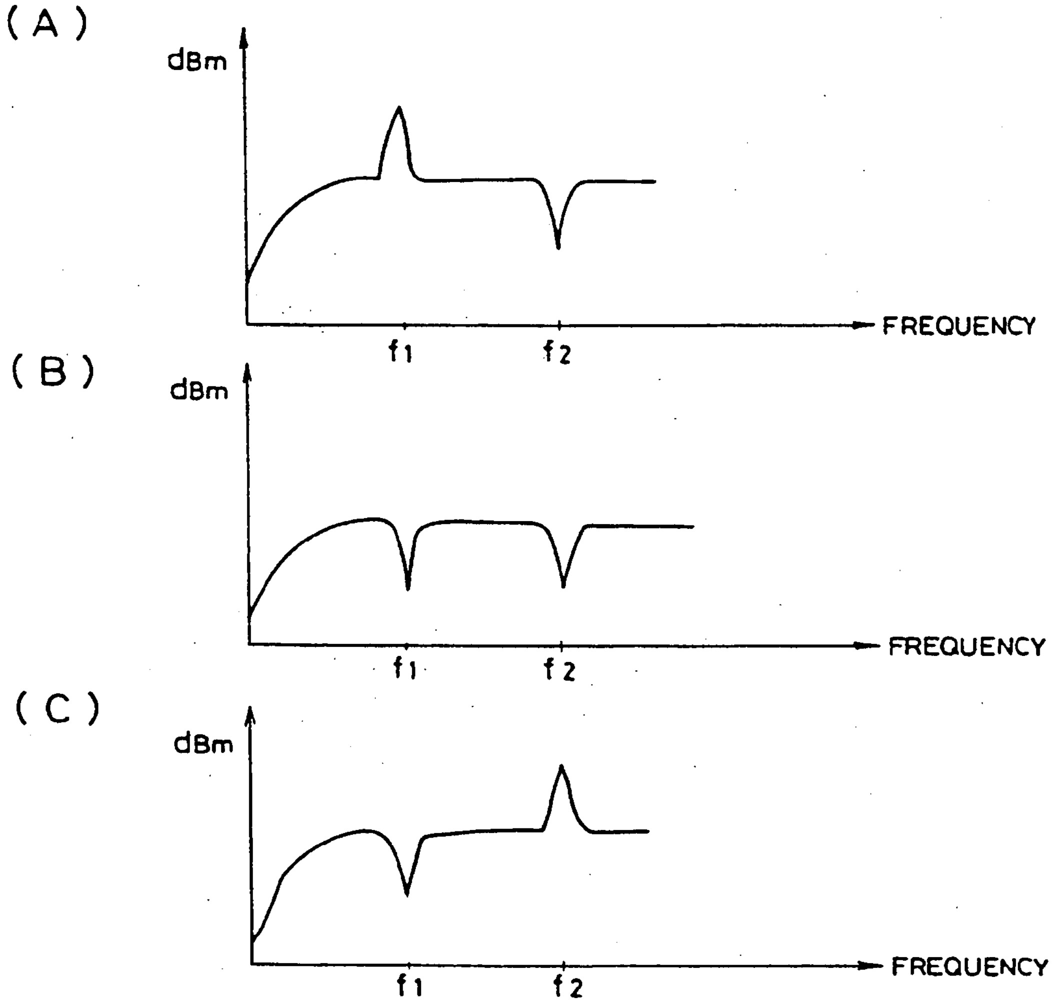
MODULATION SIGNAL 11 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0

REFERENCE CORD S0 (RUN-A) : 00 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 1 0 0 0 1 1

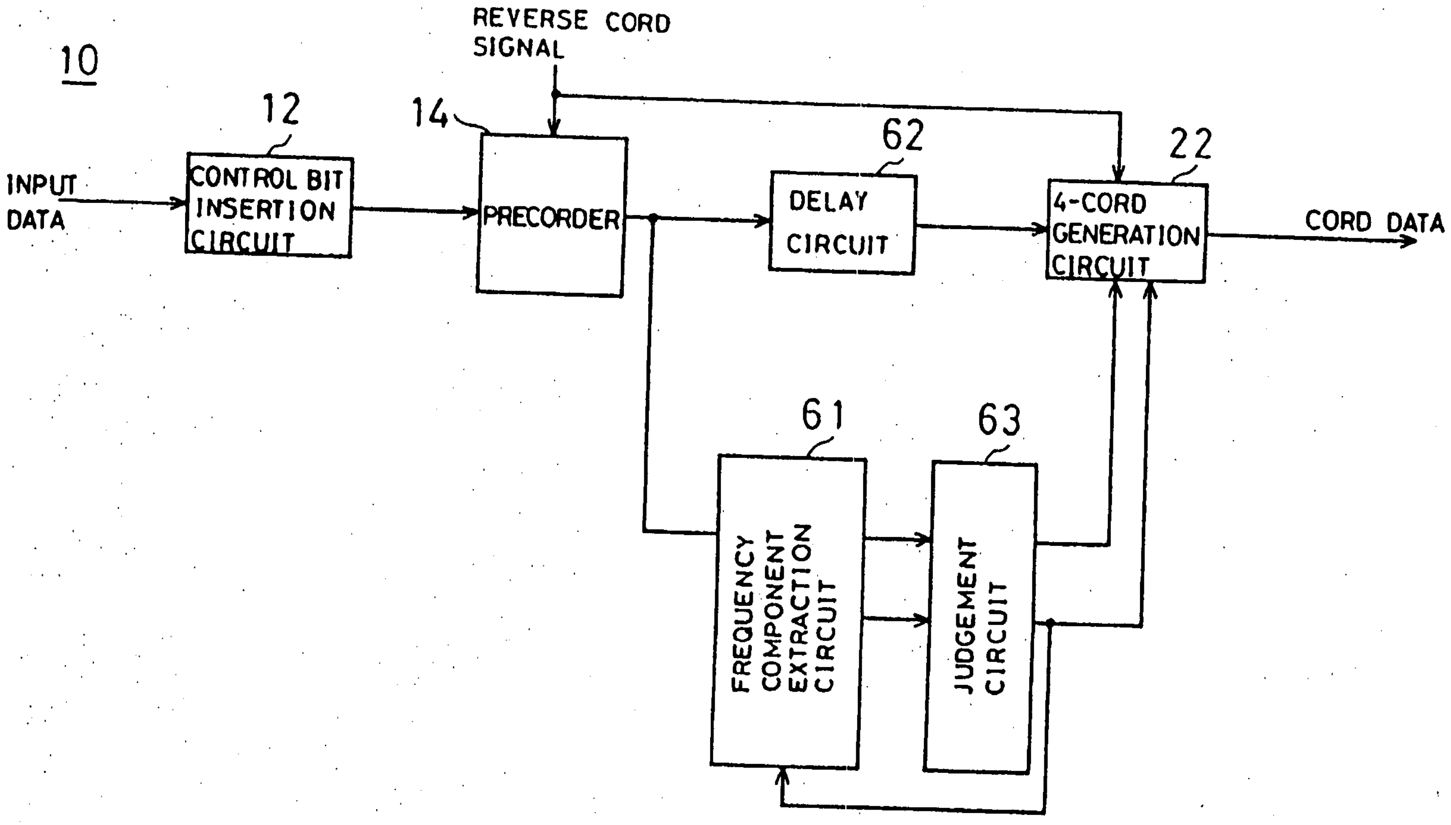
F I G.18



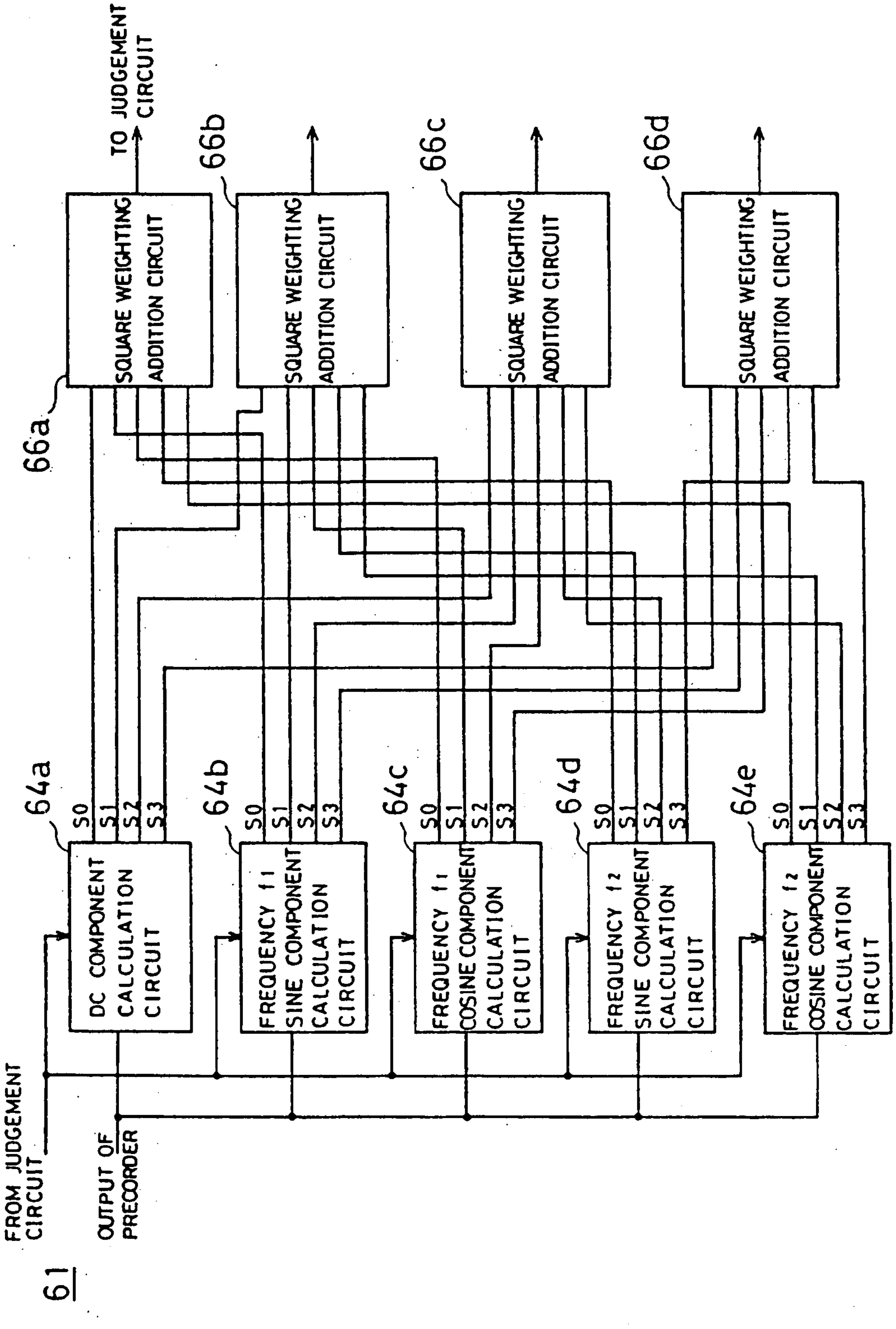
F I G. 19


(A)
dBm
FREQUENCY
f1
f2
(B)
dBm
FREQUENCY
f1
f2
(C)
dBm
FREQUENCY
f1
f2

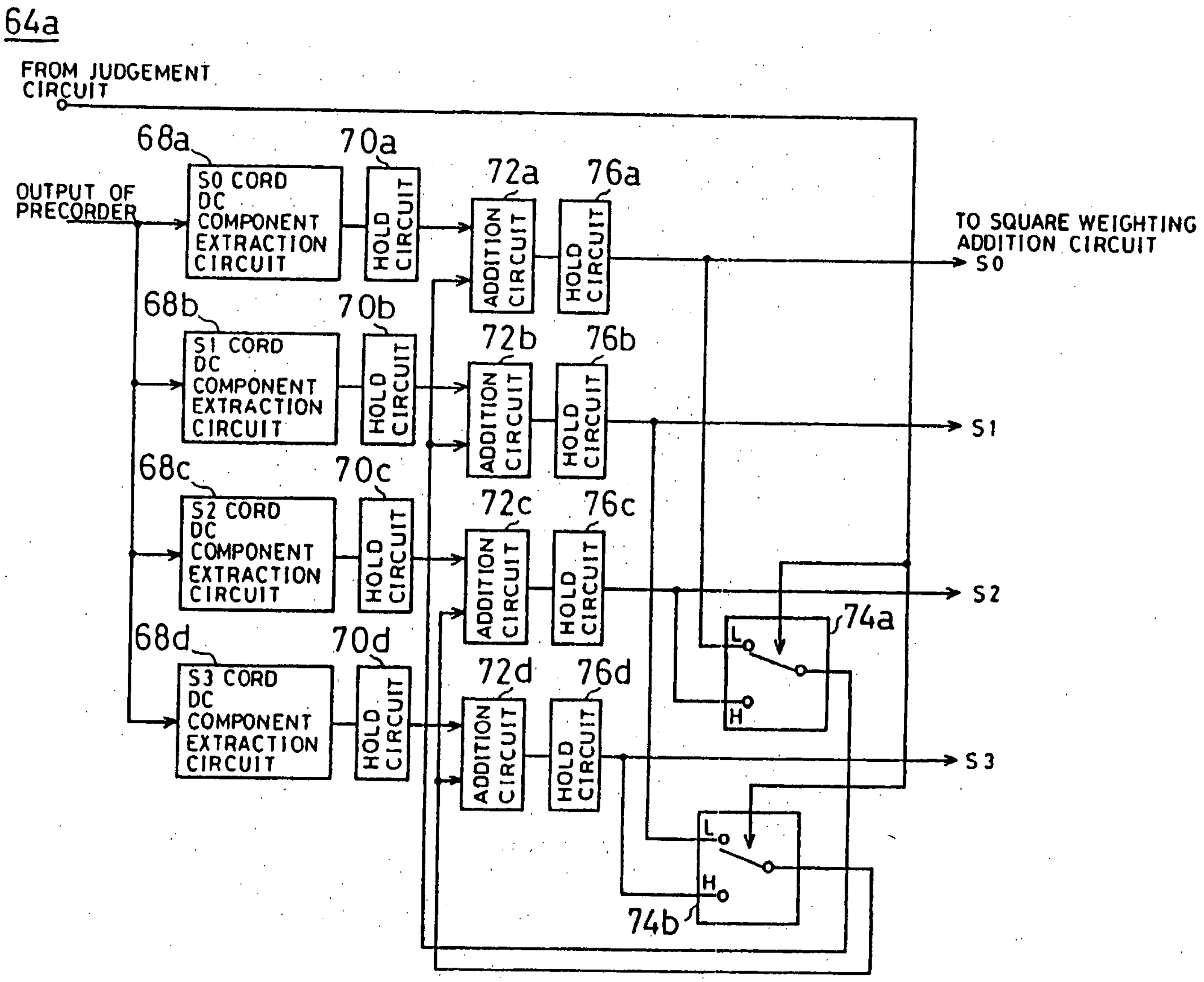
F I G. 20


10
INPUT DATA
12
CONTROL BIT INSERTION CIRCUIT
14
PRECORDER
REVERSE CORD SIGNAL
62
DELAY CIRCUIT
22
4-CORD GENERATION CIRCUIT
CORD DATA
61
FREQUENCY COMPONENT EXTRACTION CIRCUIT
63
JUDGEMENT CIRCUIT

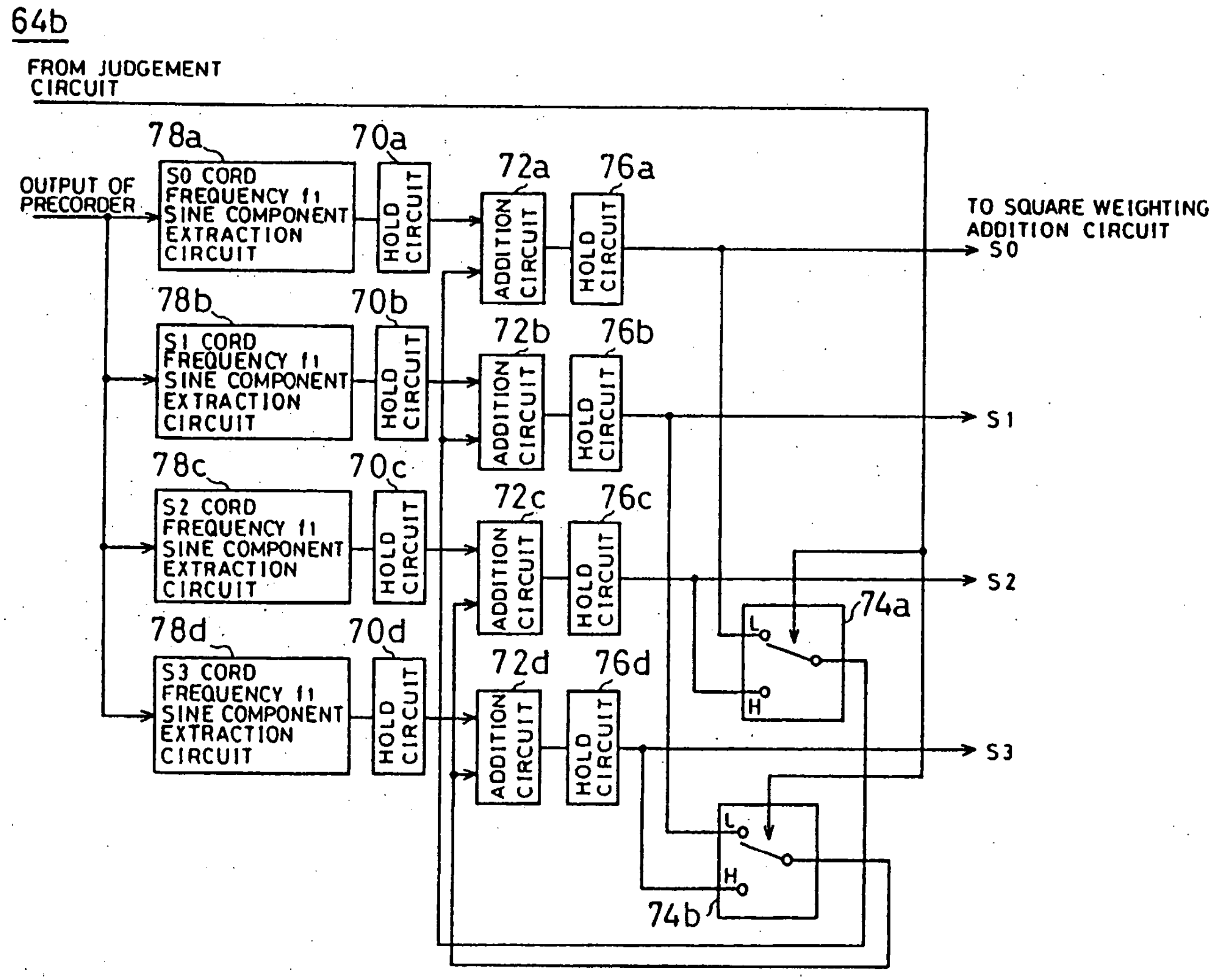
F I G. 21


61
FROM JUDGEMENT CIRCUIT
OUTPUT OF PRECORDER
64a
DC COMPONENT CALCULATION CIRCUIT
64b
FREQUENCY f1 SINE COMPONENT CALCULATION CIRCUIT
64c
FREQUENCY f1 COSINE COMPONENT CALCULATION CIRCUIT
64d
FREQUENCY f2 SINE COMPONENT CALCULATION CIRCUIT
64e
FREQUENCY f2 COSINE COMPONENT CALCULATION CIRCUIT
S0
S1
S2
S3
66a
66b
66c
66d
SQUARE WEIGHTING ADDITION CIRCUIT
TO JUDGEMENT CIRCUIT

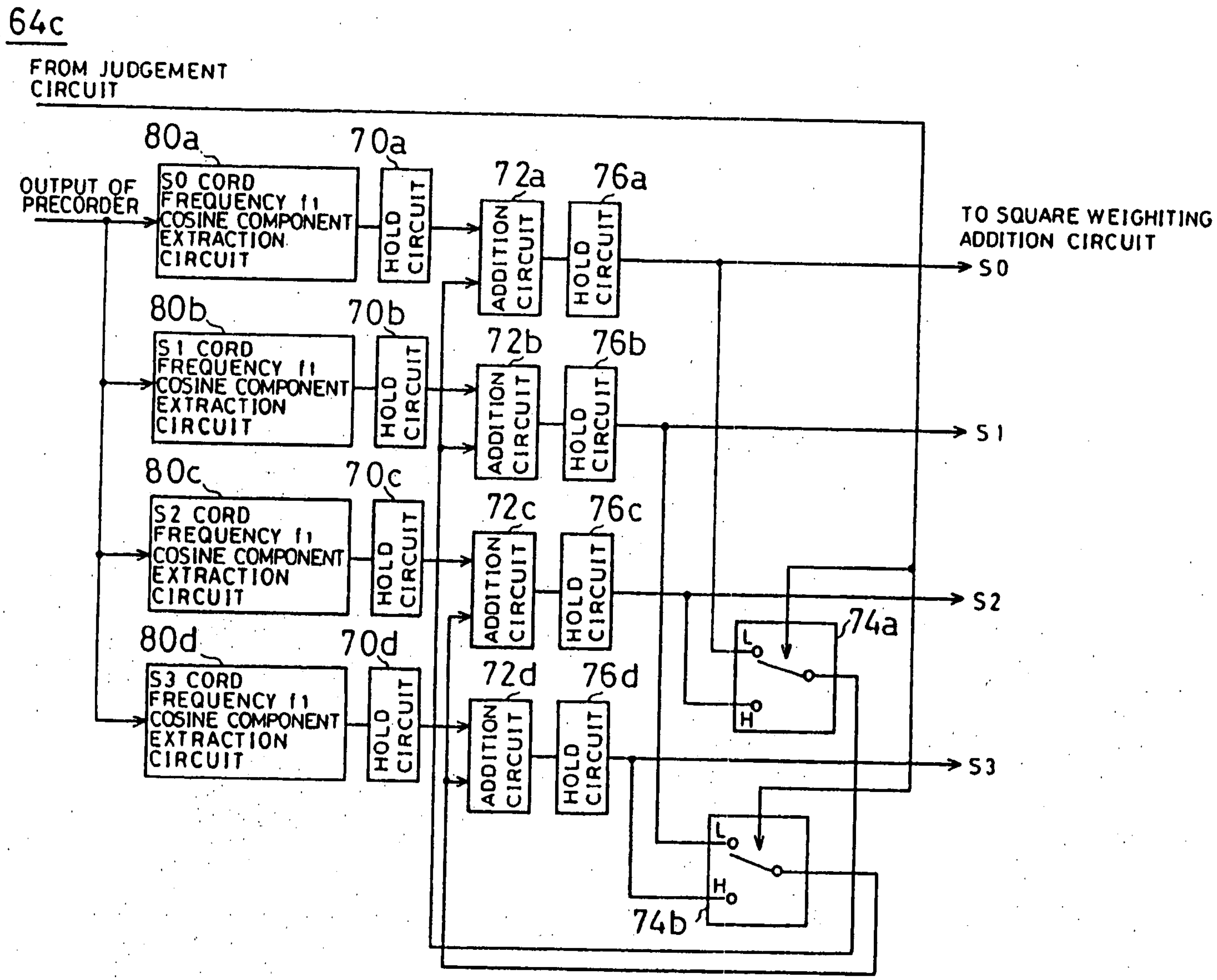
F I G. 22


64a
FROM JUDGEMENT CIRCUIT
OUTPUT OF PRECORDER
68a
S0 CORD DC COMPONENT EXTRACTION CIRCUIT
68b
S1 CORD DC COMPONENT EXTRACTION CIRCUIT
68c
S2 CORD DC COMPONENT EXTRACTION CIRCUIT
68d
S3 CORD DC COMPONENT EXTRACTION CIRCUIT
70a
70b
70c
70d
HOLD CIRCUIT
72a
72b
72c
72d
ADDITION CIRCUIT
76a
76b
76c
76d
HOLD CIRCUIT
74a
74b
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0
S1
S2
S3

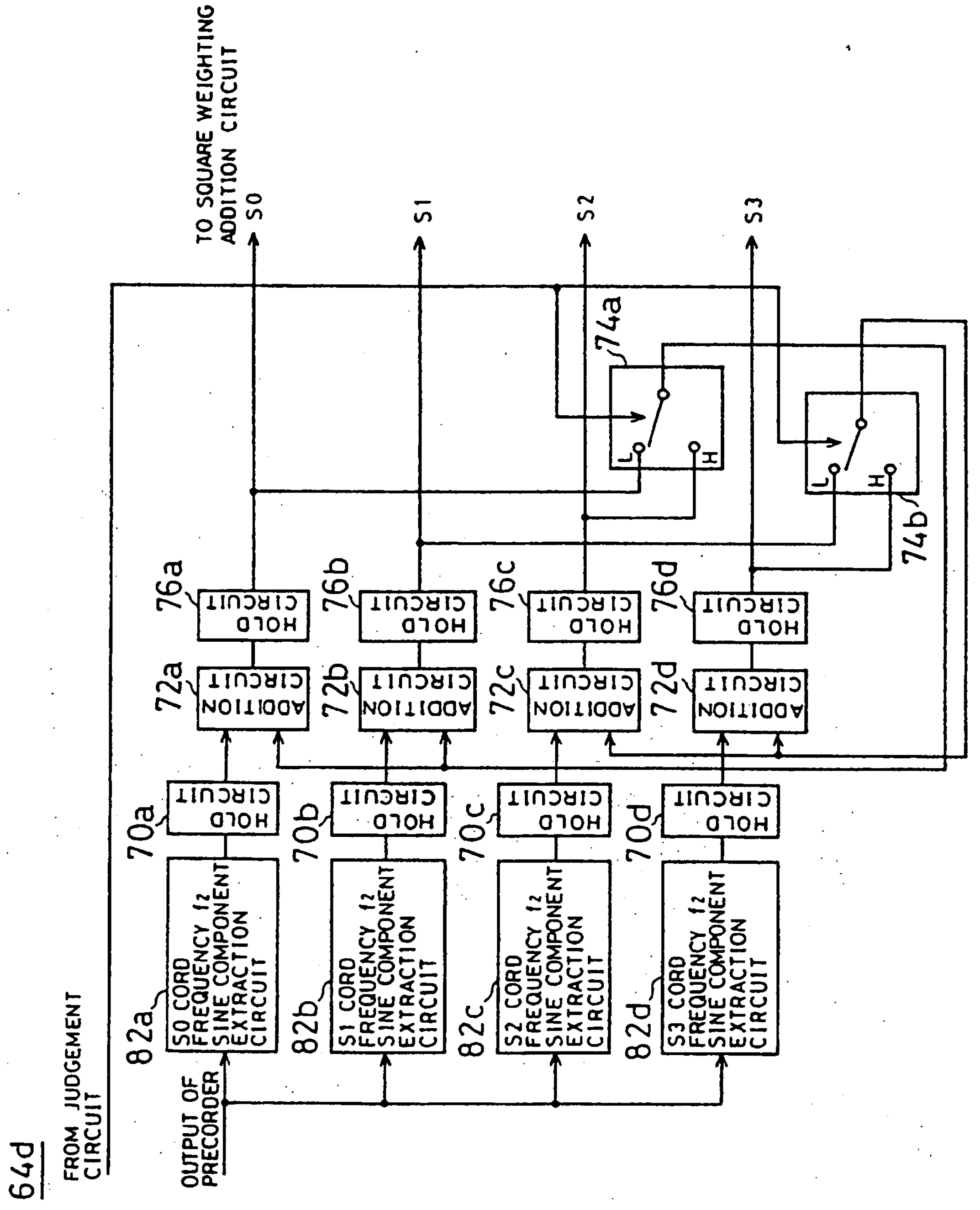
F I G. 23


64b
FROM JUDGEMENT CIRCUIT
OUTPUT OF PRECORDER
78a
S0 CORD FREQUENCY f1 SINE COMPONENT EXTRACTION CIRCUIT
78b
S1 CORD FREQUENCY f1 SINE COMPONENT EXTRACTION CIRCUIT
78c
S2 CORD FREQUENCY f1 SINE COMPONENT EXTRACTION CIRCUIT
78d
S3 CORD FREQUENCY f1 SINE COMPONENT EXTRACTION CIRCUIT
70a
70b
70c
70d
HOLD CIRCUIT
72a
72b
72c
72d
ADDITION CIRCUIT
76a
76b
76c
76d
HOLD CIRCUIT
74a
74b
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0
S1
S2
S3

F I G. 24


64c
FROM JUDGEMENT CIRCUIT
OUTPUT OF PRECORDER
80a
S0 CORD FREQUENCY f1 COSINE COMPONENT EXTRACTION CIRCUIT
80b
S1 CORD FREQUENCY f1 COSINE COMPONENT EXTRACTION CIRCUIT
80c
S2 CORD FREQUENCY f1 COSINE COMPONENT EXTRACTION CIRCUIT
80d
S3 CORD FREQUENCY f1 COSINE COMPONENT EXTRACTION CIRCUIT
70a
70b
70c
70d
HOLD CIRCUIT
72a
72b
72c
72d
ADDITION CIRCUIT
76a
76b
76c
76d
HOLD CIRCUIT
74a
74b
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0
S1
S2
S3

F I G. 25


64d
FROM JUDGEMENT CIRCUIT
OUTPUT OF PRECORDER
82a
S0 CORD FREQUENCY f2 SINE COMPONENT EXTRACTION CIRCUIT
82b
S1 CORD FREQUENCY f2 SINE COMPONENT EXTRACTION CIRCUIT
82c
S2 CORD FREQUENCY f2 SINE COMPONENT EXTRACTION CIRCUIT
82d
S3 CORD FREQUENCY f2 SINE COMPONENT EXTRACTION CIRCUIT
70a
HOLD CIRCUIT
70b
HOLD CIRCUIT
70c
HOLD CIRCUIT
70d
HOLD CIRCUIT
72a
ADDITION CIRCUIT
72b
ADDITION CIRCUIT
72c
ADDITION CIRCUIT
72d
ADDITION CIRCUIT
76a
HOLD CIRCUIT
76b
HOLD CIRCUIT
76c
HOLD CIRCUIT
76d
HOLD CIRCUIT
74a
L
H
74b
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0
S1
S2
S3

F I G. 26

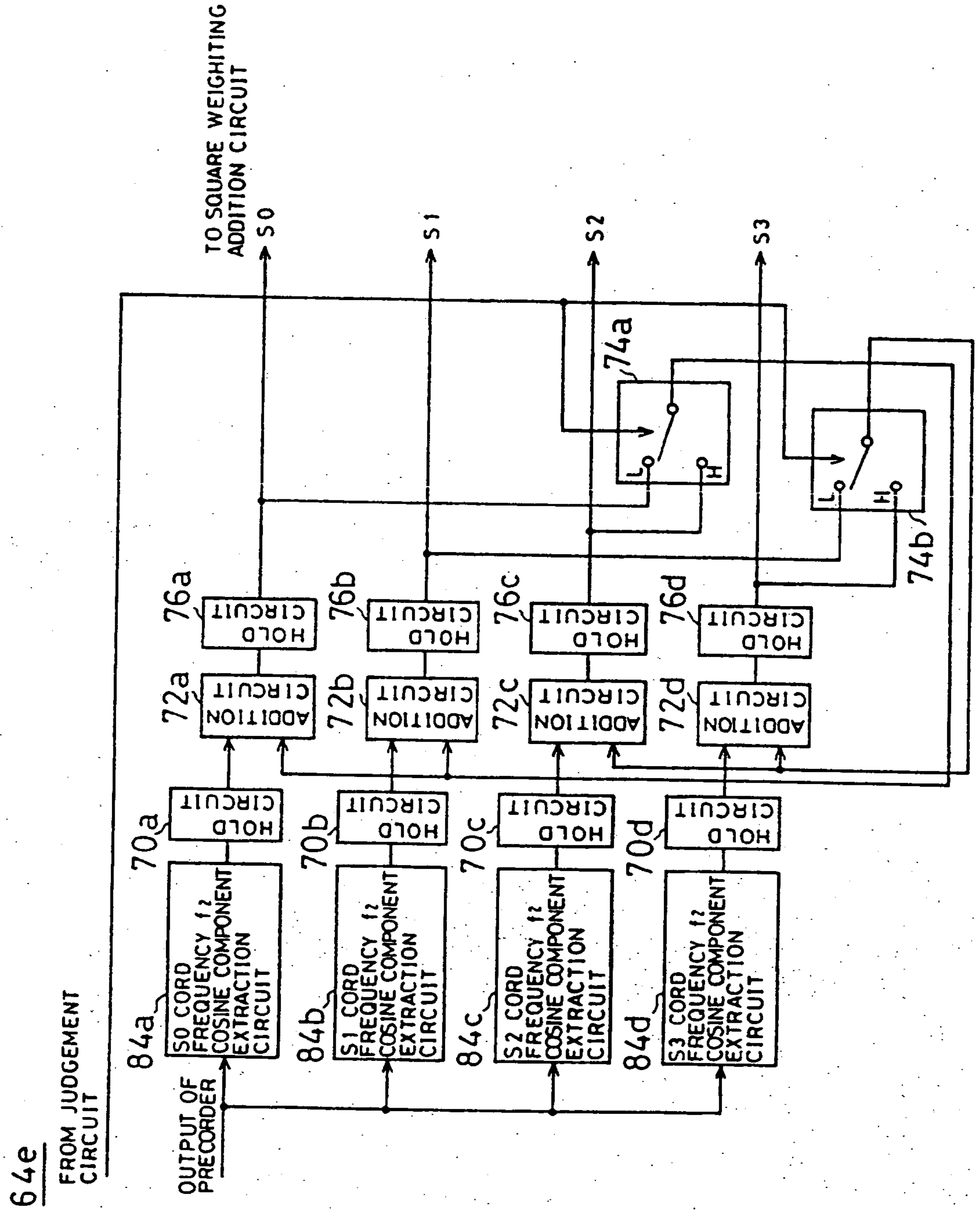
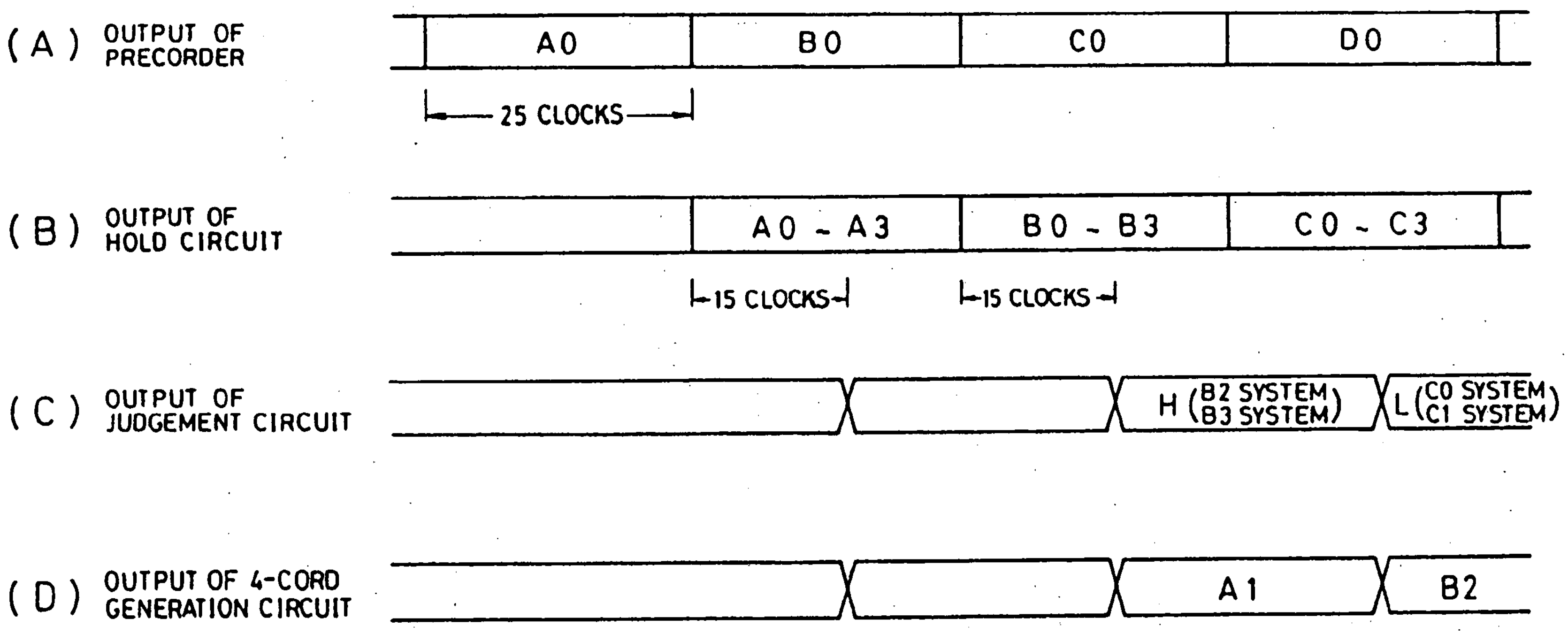

64e
FROM JUDGEMENT CIRCUIT
OUTPUT OF PRECORDER
84a
S0 CORD FREQUENCY f2 COSINE COMPONENT EXTRACTION CIRCUIT
84b
S1 CORD FREQUENCY f2 COSINE COMPONENT EXTRACTION CIRCUIT
84c
S2 CORD FREQUENCY f2 COSINE COMPONENT EXTRACTION CIRCUIT
84d
S3 CORD FREQUENCY f2 COSINE COMPONENT EXTRACTION CIRCUIT
70a
HOLD CIRCUIT
70b
HOLD CIRCUIT
70c
HOLD CIRCUIT
70d
HOLD CIRCUIT
72a
ADDITION CIRCUIT
72b
ADDITION CIRCUIT
72c
ADDITION CIRCUIT
72d
ADDITION CIRCUIT
76a
HOLD CIRCUIT
76b
HOLD CIRCUIT
76c
HOLD CIRCUIT
76d
HOLD CIRCUIT
74a
L
H
74b
L
H
TO SQUARE WEIGHTING ADDITION CIRCUIT
S0
S1
S2
S3

FIG. 27


(A) OUTPUT OF PRECORDER
A0
B0
C0
D0
25 CLOCKS
(B) OUTPUT OF HOLD CIRCUIT
A0 ~ A3
B0 ~ B3
C0 ~ C3
15 CLOCKS
15 CLOCKS
(C) OUTPUT OF JUDGEMENT CIRCUIT
H (B2 SYSTEM B3 SYSTEM)
L (C0 SYSTEM C1 SYSTEM)
(D) OUTPUT OF 4-CORD GENERATION CIRCUIT
A1
B2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP95/01951

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl^6 G11B20/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int. Cl^6 G11B20/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1955 - 1995
Kokai Jitsuyo Shinan Koho	1971 - 1995

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 6-131822, A (Matsushita Electric Ind. Co., Ltd.), May 13, 1994 (13. 05. 94) & EP, 593173, A	1 - 11
A	JP, 5-284035, A (Sony Corp.), October 29, 1993 (29. 10. 93) (Family: none)	1 - 11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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Date of the actual completion of the international search January 8, 1996 (08. 01. 96)	Date of mailing of the international search report January 30, 1996 (30. 01. 96)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)